



## 2022 반도체전공트랙 간담회

# 지능형 반도체 소자 및 집적회로 연구실 (*i*-S!LK)

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School of Electrical Engineering,  
Kookmin University

지도교수: 김대환, 최성진, 배종호, 김동명

# Professor



**Prof. Dong Myong Kim, Ph.D.**

- ✓ Seoul National University, BSEE, (1986. 2.)
- ✓ Seoul National University, MSEE, (1988. 2.)
- ✓ University of Minnesota (Government scholarship), Ph.D.EE, (1993. 2.)
- ✓ Korea Institute of Science and Technology(KIST), Researcher, (1988. 2. - 1989. 8.)
- ✓ School of Electrical Eng., Kookmin Univ., Professor, (1993. 3. ~ )



**Prof. Sung-Jin Choi, Ph.D.**

- ✓ Chung-Ang University, BSEE, (2007. 2.)
- ✓ KAIST, MSEE, (2008. 8.)
- ✓ KAIST, Ph.D.EE, (2012. 2.)
- ✓ ETRI: Electronics and Telecommunications Research Institute, Assistant researcher (2009. 1 ~ 2011. 1)
- ✓ University of California, Berkeley (PI: Prof. Jeffrey Bokor), Postdoctoral researcher (2011. 12 ~ 2013. 2)
- ✓ School of Electrical Eng., Kookmin Univ., Associate Professor (2013. 2. ~ )



**Prof. Dae Hwan Kim, Ph.D.**

- ✓ Seoul National University, BSEE, (1996. 2.)
- ✓ Seoul National University, MSEE, (1998. 2.)
- ✓ Seoul National University, Ph.D.EE, (2002. 2.)
- ✓ Semiconductor Materials and Device Laboratory(SMDL) in Seoul National University, Postdoctoral researcher, (2002. 3. - 2002. 8.)
- ✓ Samsung Electronics, DRAM Design Team, Principal Research Engineer, (2002. 9. - 2005. 8.)
- ✓ University of Michigan, Ann Arbor,
- ✓ USA Visiting Scholar , (2012. 3. - 2013. 2.)
- ✓ School of Electrical Eng., Kookmin Univ., Professor (2005. 9. ~ )



**Prof. Jong-Ho Bae, Ph.D.**

- ✓ Pohang University of Science and Technology, BSEE, (2011. 2.)
- ✓ Seoul National University, Ph.D.EE, (2018. 2.)
- ✓ Inter-university Semiconductor Research Center in Seoul National University, Assistant researcher, (2018. 3. - 2019. 7.)
- ✓ University of California, Berkeley (PI: Prof. Sayeef Salahuddin), Postdoctoral researcher (2019. 7 ~ 2020. 7)
- ✓ School of Electrical Eng., Kookmin Univ., Assistant Professor (2020. 9. ~ )

# Vision

## 다양한 연구 장려제도

- 삼성전자 · LG Display · SK Hynix 산학 협력을 통한 입사 추천!
- 등록금 지원
- 삼성전자 휴먼테크 논문대상 9회 (삼성전자 입사 특전)
- 박사과정 진학 권장 / 지원 (S!LK, 문부성 장학생, 미국유학 등)
- 연구과제 수행 - 졸업논문 주제의 연관성 최대한 확보
- 외국 대학 internship 제도 활용 지원

## S!LK 졸업자 현황 (전체)

- 삼성전자/디스플레이 : 48명
- SK Hynix/SKC : 10명
- LG display/Innotek/SiliconWorks : 26명
- DB HiTek : 8명
- 외국기업(Intel / IBM / BOE) : 3명
- 대학/연구소 : 2명
- Magnachip/SEMES : 3명
- 기타 : 18명

## 교육 Plan

- 탄탄한 기초 이론
- 실용적인 실험/분석 능력 배양
- 반도체 소자 기초 이론에서부터, 최신 기술 수준까지 Cover

## ~22' S!LK 실적

SCI급 국제 저널 **407**편  
특허 **72**건  
국내/국외 학회 발표 **314**회  
수상 **33**회

## <최근 졸업생>

삼성전자 (9) LG Display (10)  
SK Hynix (4) DB HiTek (4)  
LX 세미콘 SEMES  
S!LK 박사과정 진학 (4)

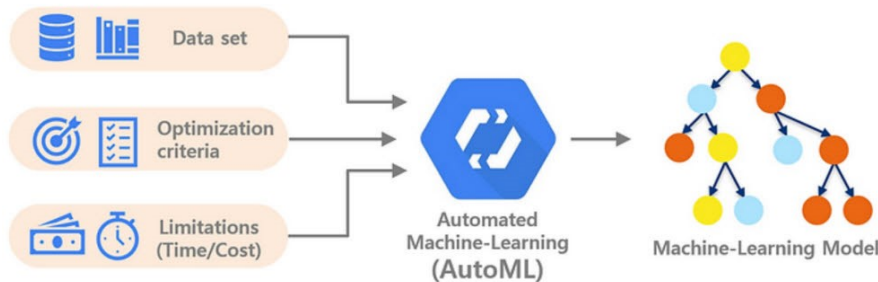
- 높은 취업률과 연구 성과 (평균 SCI(E) 논문 주저자 2.6편 + 공동저자 5.3편)
- 예비 석사 제도 – 석박사 진학 예정자 / 체계적인 교육 / 맞춤형 멘토-멘티 시스템

BK21 4단계, ERC(C-ICT 연구센터), 지능형반도체 관련 국책 과제 진행 중 (7개)

삼성전자/LG Display 외, 다양한 대/중소기업과 활발한 협업 (실용적 기술 지향)

# Industry-University Co-op Project

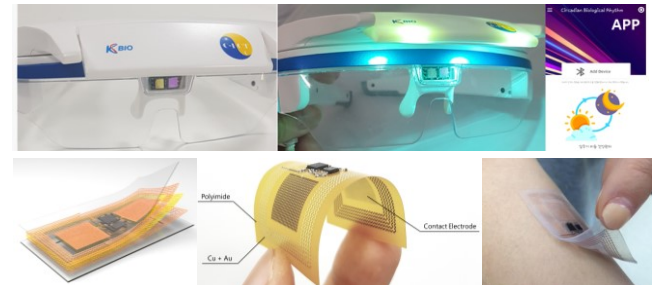
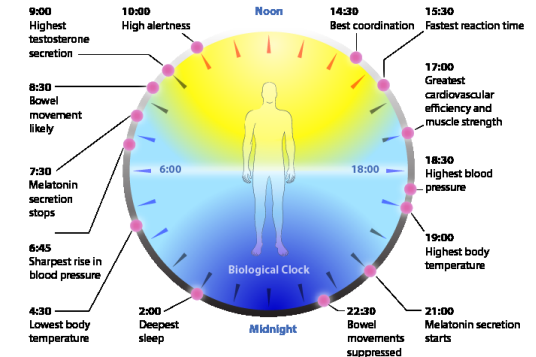
반도체전공트랙 참여기업과의 산학협력 연구 (진행 중)



## 인공지능 기반 반도체 소자 모델링

- 반도체 소자 측정/분석, 모델링
- 반도체 모델링/EDA Tool 개발/개선 (Alsys 2.0)
- 인공지능 모델 (AI 모델) 개발/개선

그 외 반도체전공트랙 참여기업으로  
산학협력 프로젝트 확대 계획



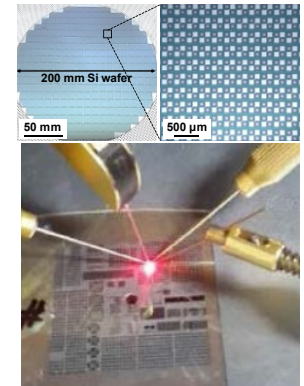
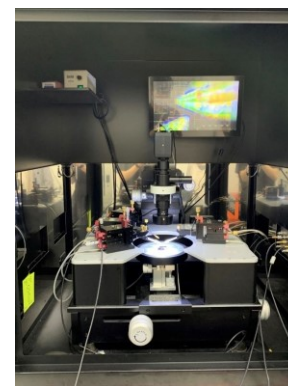
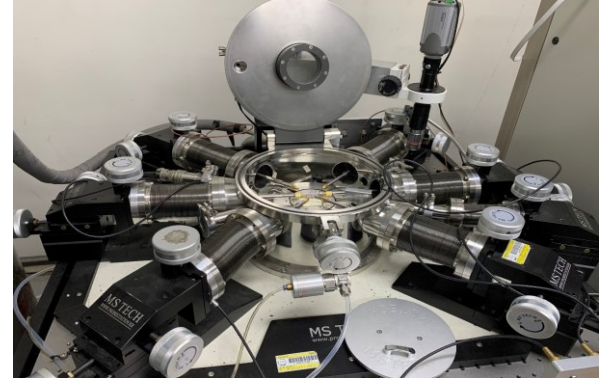
## 씨카디언 리듬 조절을 위한 스마트 IoT시스템 (스마트 IoT 기기 및 스마트 홈 시스템)

- 지능형 반도체 설계 (소자/회로/시스템 수준)
- 스마트 센서 설계 (소자/구동회로/시스템 수준)
- 스마트 IoT 기기 및 시스템

→ 연구 경험 / 연구 참여 Chance!



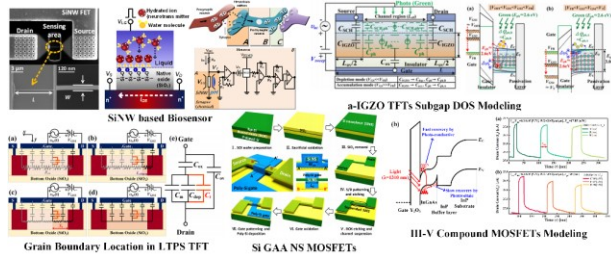
# Research Environment



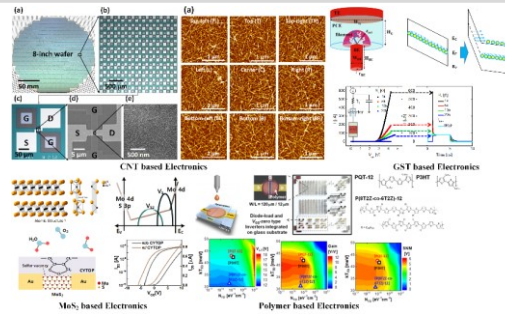
- 반도체 소자/회로 제작 (K-Fab. (클린룸), 산학협력관 5층)
- 측정/분석 시스템 구축
- 매 학기 self-user 교육 후 (대학원생), 직접 장비 사용의 기회

# Research Field of S!LK

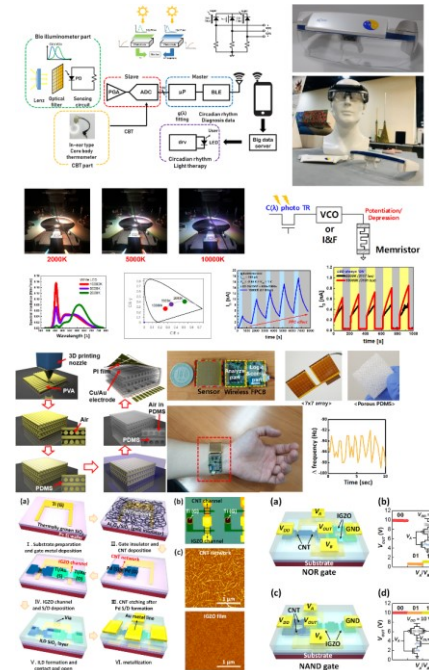
## CMOS device and integrated circuits



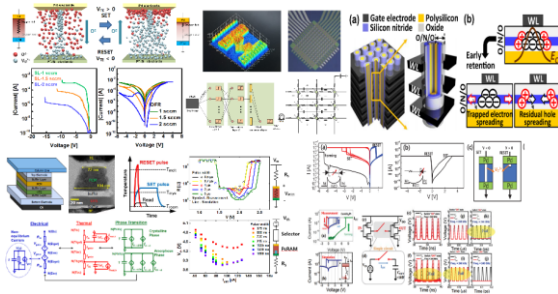
## Emerging materials-based electronics



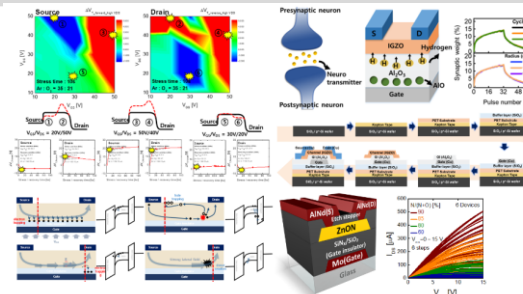
## Hybrid device-based circadian ICT research center



## Future Memory



## Oxide materials-based electronics (Display)



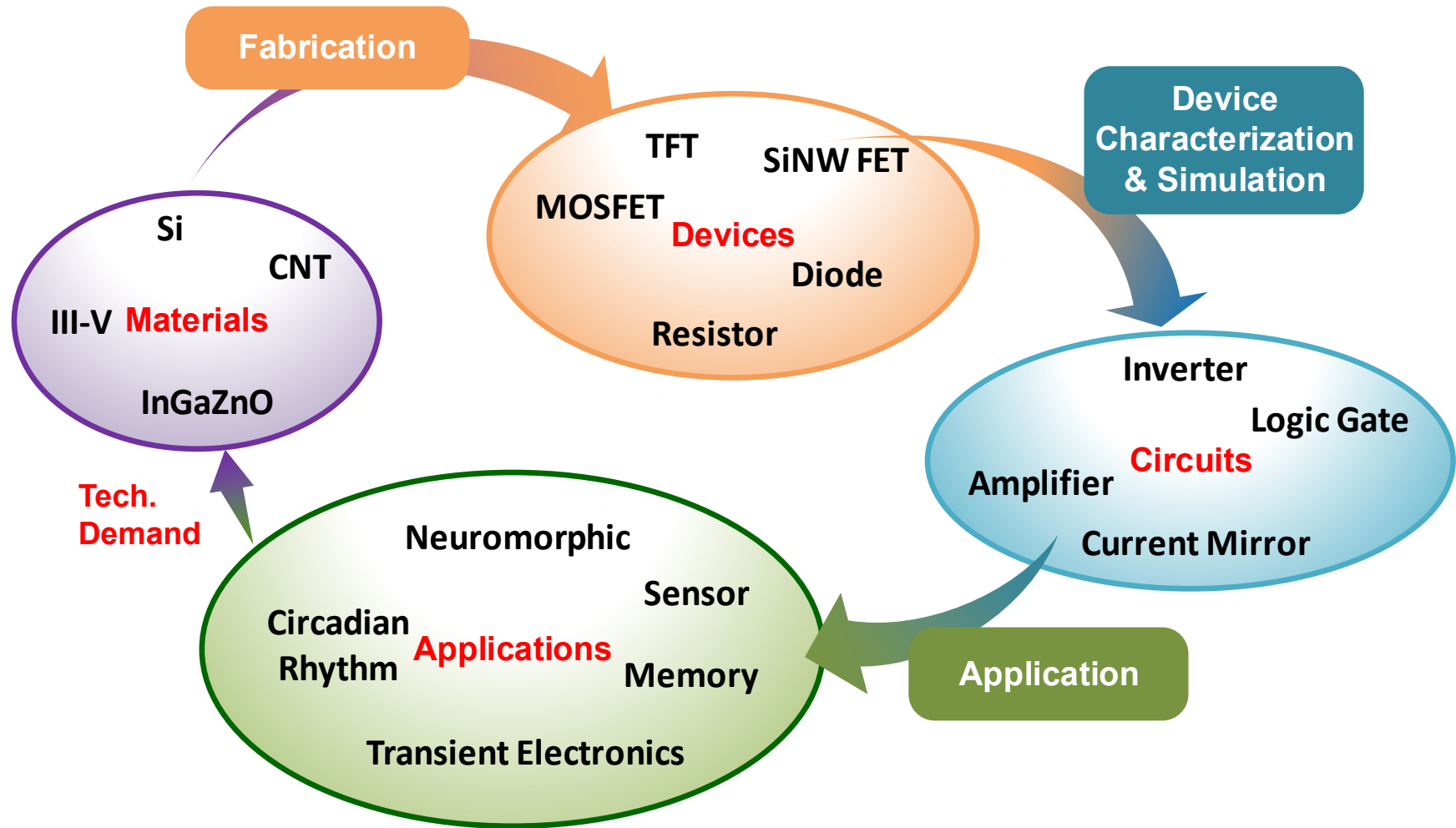
- 반도체 소자/회로/시스템 - 재료/구조/공정 설계/제작(공정) → 분석/모델링
- 반도체 응용 기술 연구 - 차세대 메모리/로직 반도체, 센서, 디스플레이, IoT 기기 등

→ (1) 새로운 응용 개발

→ (2) 개선점 발견 → 재료/소자 개발 (순환)

반도체 재료/소자 구조 개발 → 분석/모델링

# Research Direction of S!LK



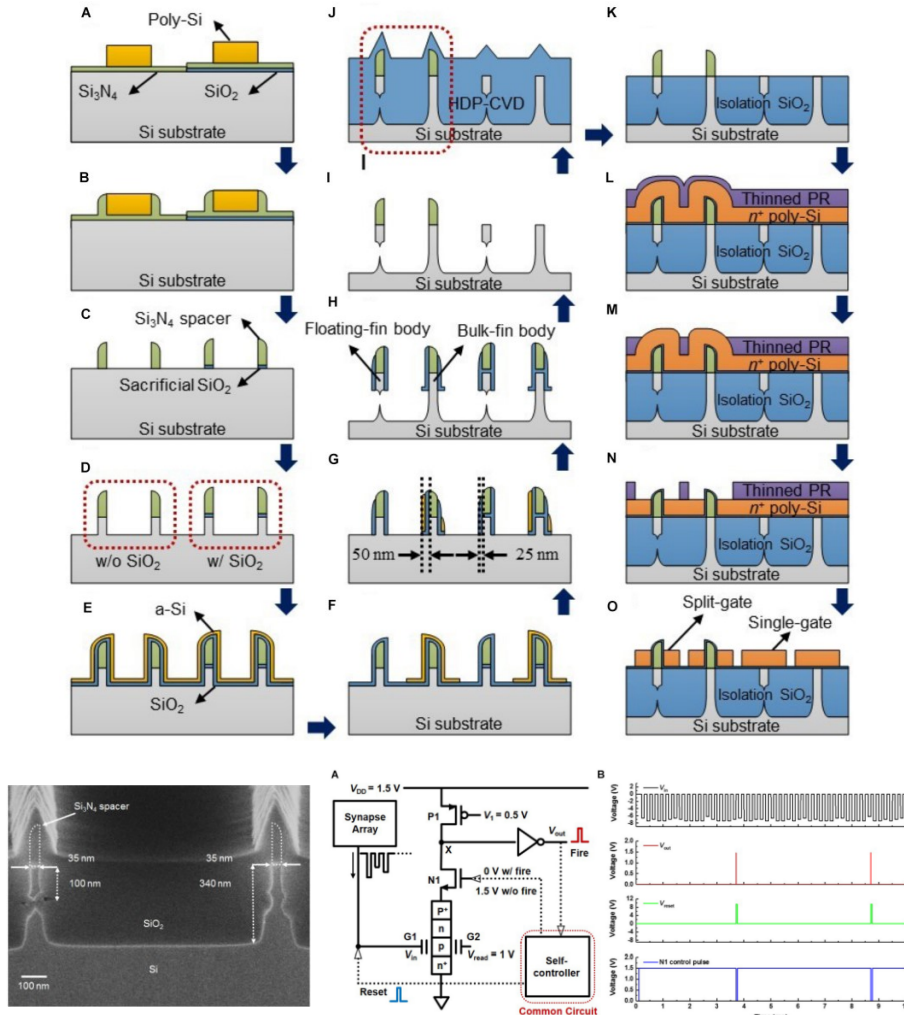
반도체 기본(재료, 이론, 공정) → 응용 (반도체 기술 전반)



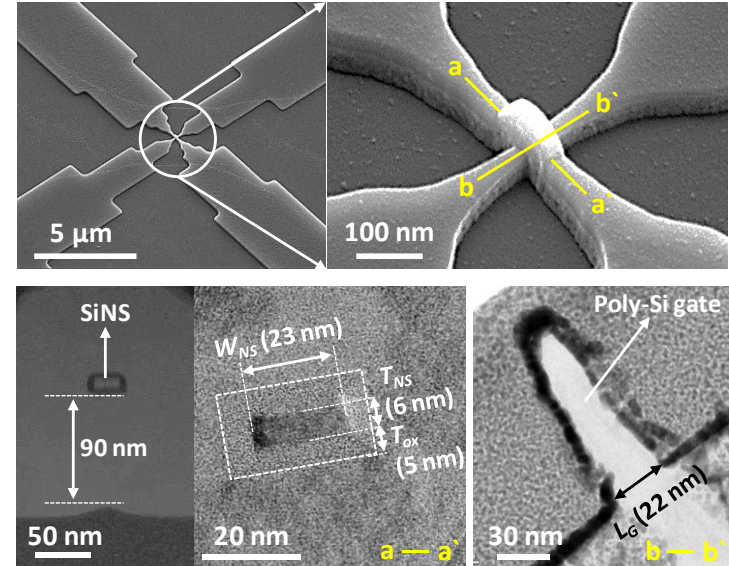
# Device Fabrication

## Device/CMOS Circuit Design & Fabrication, Process Design

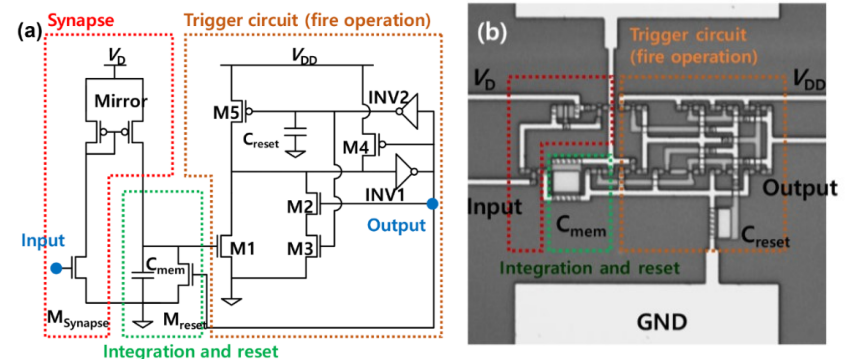
### ➤ Fabrication Process Design (공정 설계/제작) 'New Device'–CMOS Circuit Cointegration



### ➤ GAAFET (NNFC)



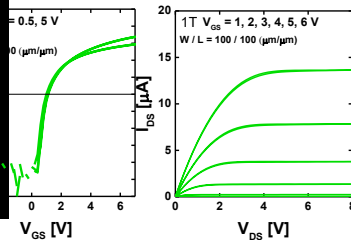
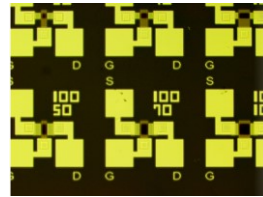
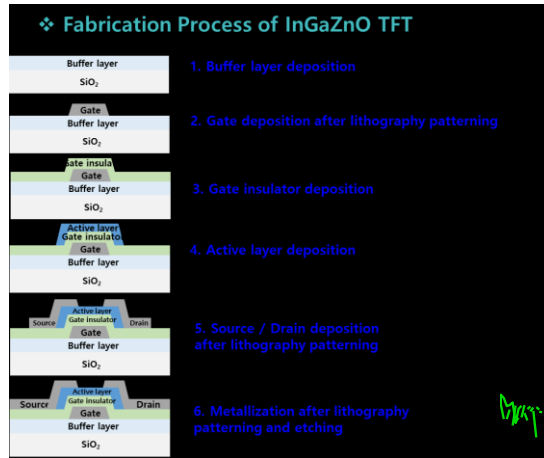
### ➤ Si CMOS Circuits for AI (ISRC) (Processing-In-Memory, PIM)



# Device Fabrication in K-Fab.

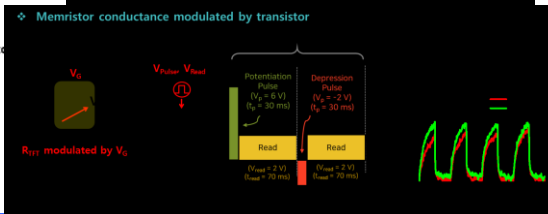
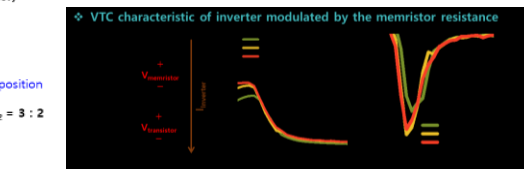
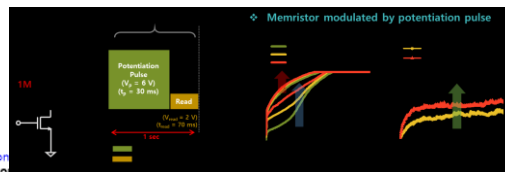
## (Display, Memory)

### ➤ IGZO TFT Fabrication



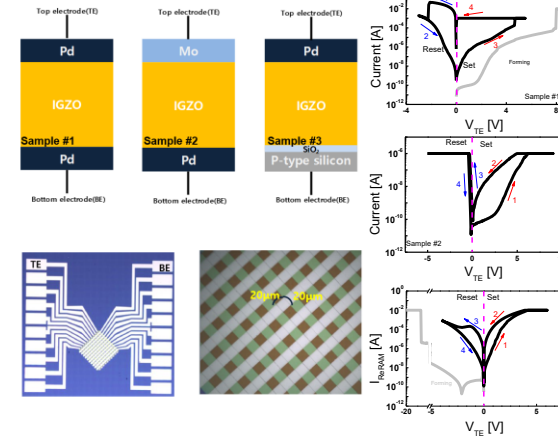
### ➤ 1T1M(1Transistor 1Memristor) Fabrication

#### ❖ Fabrication Process of InGaZnO TFT and InGaZnO memristor



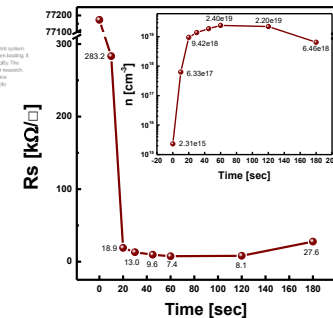
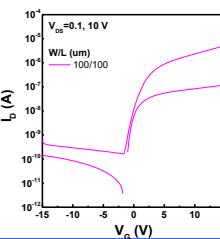
### ➤ ReRAM, Memristor Array Fabrication

- ❖ Pd/IGZO/Pd, Mo/IGZO/Pd**
- SiO<sub>2</sub> (300 nm) oxidation wafer
  - Bottom electrode deposition  
→ E-beam evaporator (Ti: 2nm, Pd: 40 nm)
  - IGZO deposition  
→ Sputter (Ar: O<sub>2</sub> = 3 : 2 sccm, RF power = 150W,  $\approx 60nm$ )
  - Top electrode deposition  
→ E-beam evaporator (Ti: 2nm, Pd: 40 nm): Sample #1  
→ E-beam evaporator (Ti: 2nm, Mo: 40 nm): Sample #2



### ➤ IGZO TFT with Top Gate Self Aligned Coplanar Structure Fabrication.

SiO<sub>2</sub> (150 nm) – Etching Rate: 54.7 nm / min  
3 min (2 min + 1 min)  
[IGZO (Doping)]  
20 sec

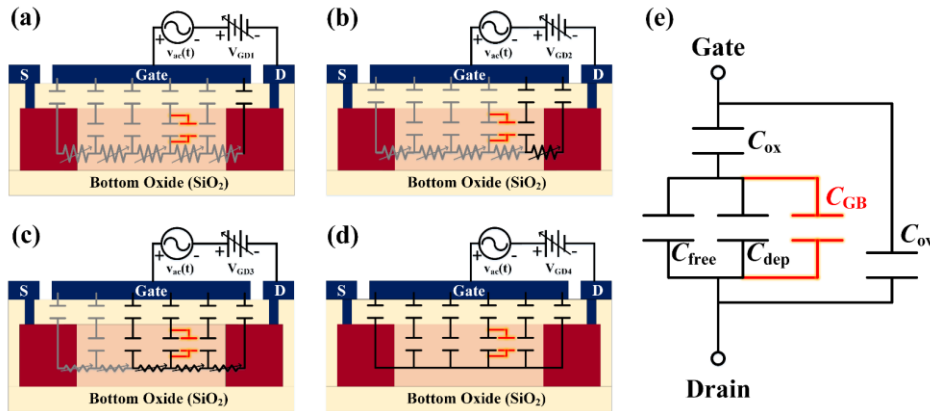


# Device Modeling and Characterization

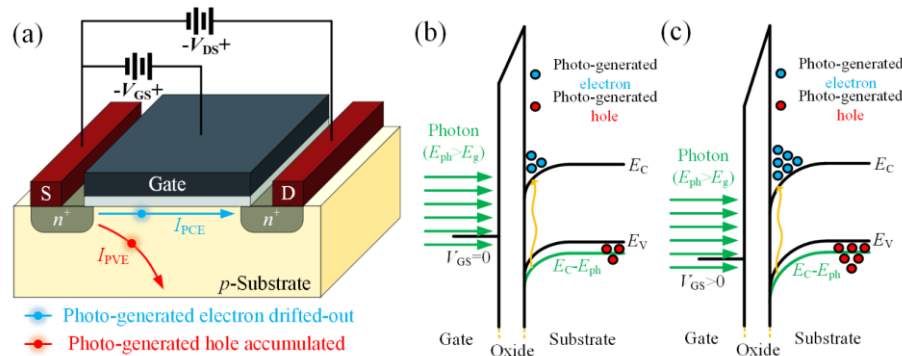
(Analysis on Generic Devices—Memory, Logic Tr., Display Tr., etc.)

## ❖ Modeling and Characterization of CMOS device using opto-electronic characteristics.

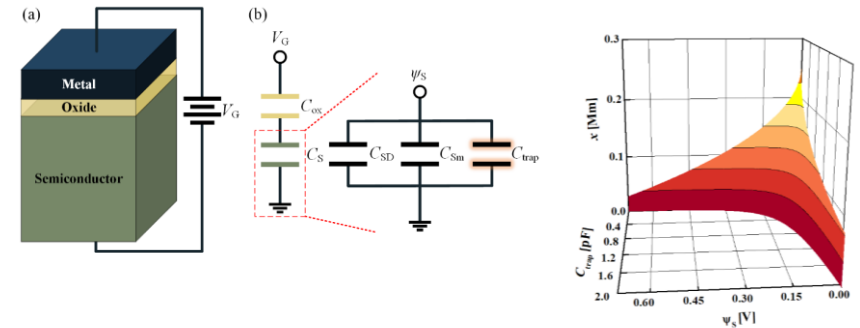
### ➤ Characterization of Grain Boundary Trap



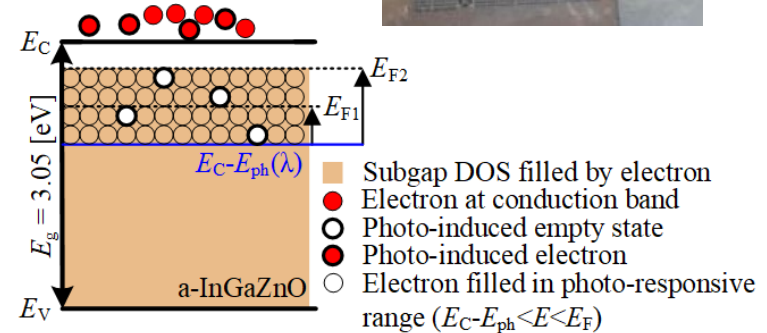
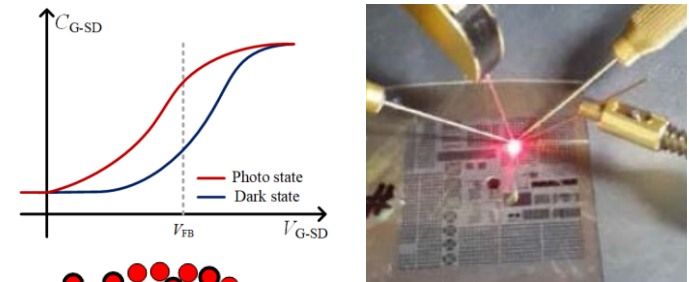
### ➤ Modeling of photonic response in MOSFETs



### ➤ Extraction of trap in MOS structure



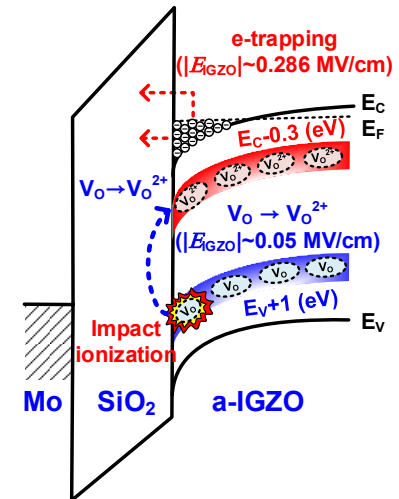
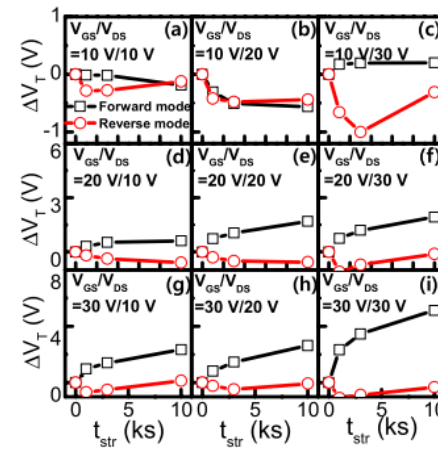
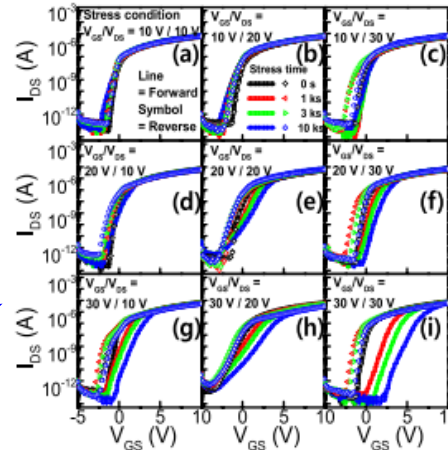
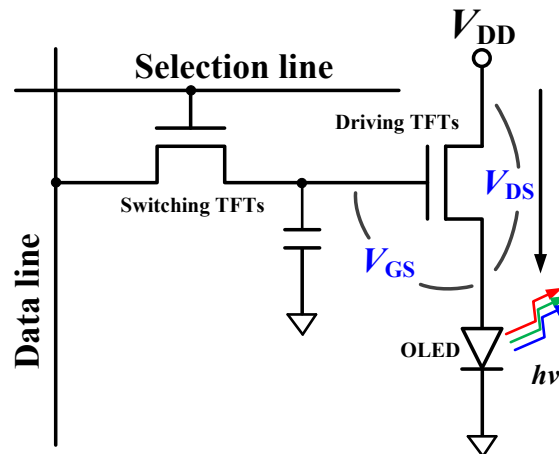
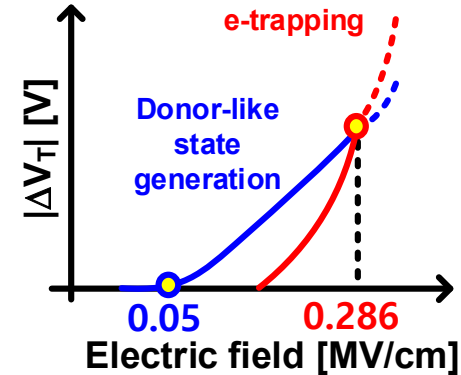
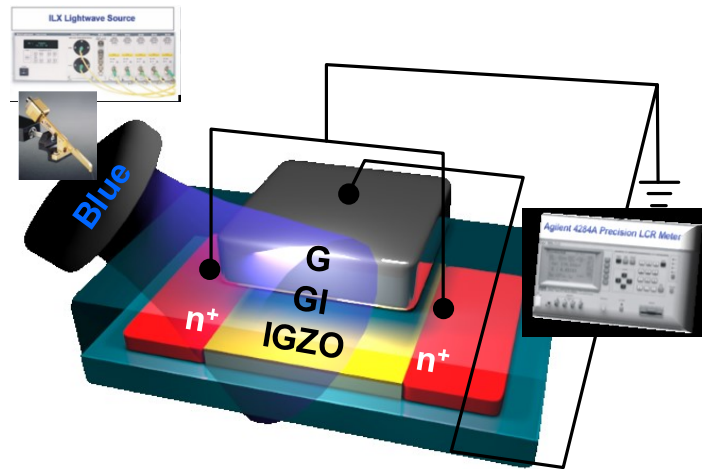
### ➤ Extraction of trap using opto-electronic technique





# Device Modeling and Characterization

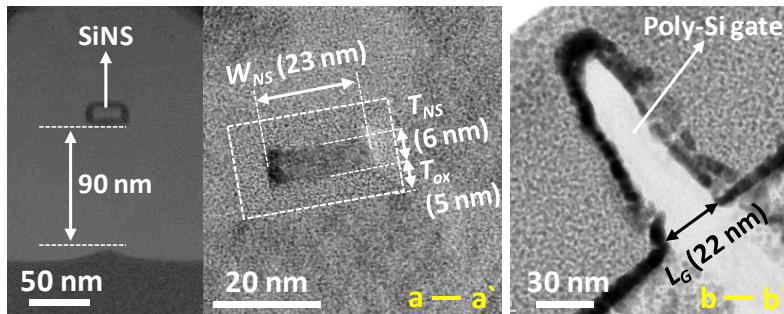
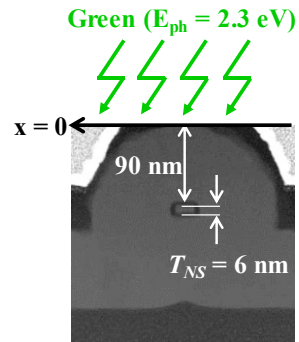
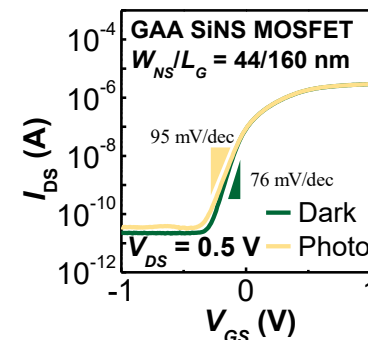
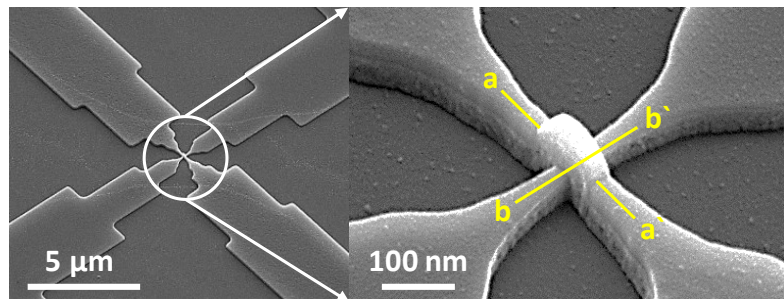
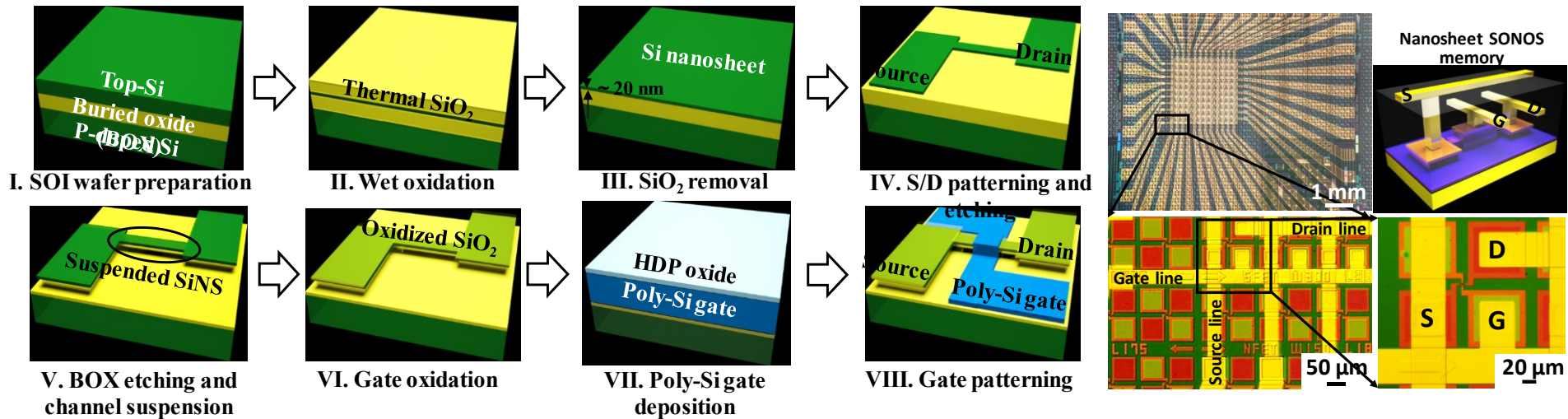
## (Analysis on Display Devices)



➔ **Transparent/Flexible Display: Instability under OLED operation**



# Logic: Gate-All-Around Si Nanosheet MOSFETs

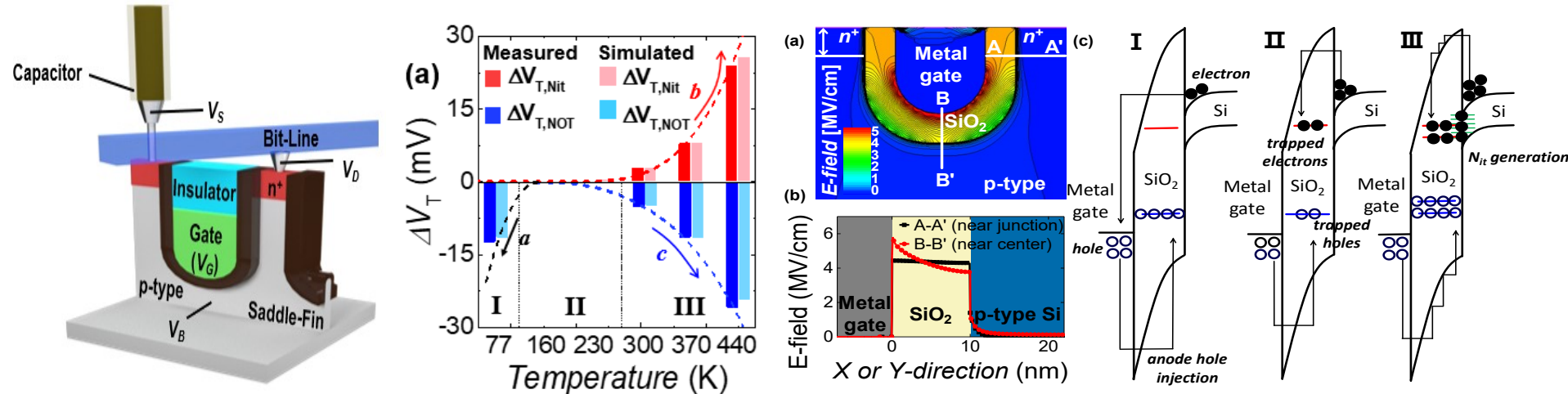


$$m_{photo} - m_{dark} = \Delta m(V_{GS}) = \frac{C_{photo}(V_{GS})}{C_{ox}}$$

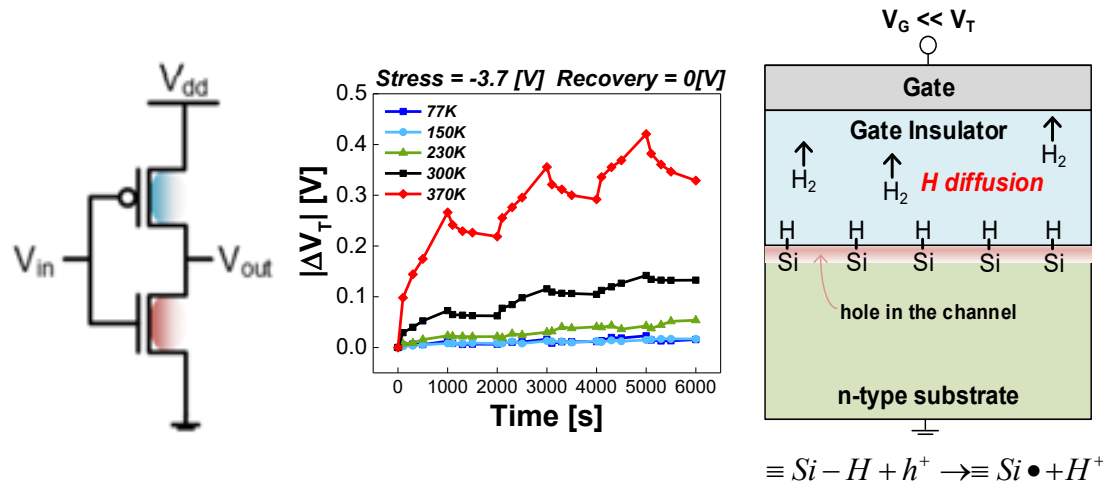
$$C_{photo}(\psi_s) = C_{ox} \int_{\psi_s(V_{GS})}^{\psi_s(V_{GS} + \Delta V_{GS})} \frac{d\Delta m(V_{GS})}{dV_{GS}} \cdot \left( \frac{d\psi_s}{dV_{GS}} \right)^{-1} d\psi_s$$

# Memory: DRAM Cell TR, Peri TR

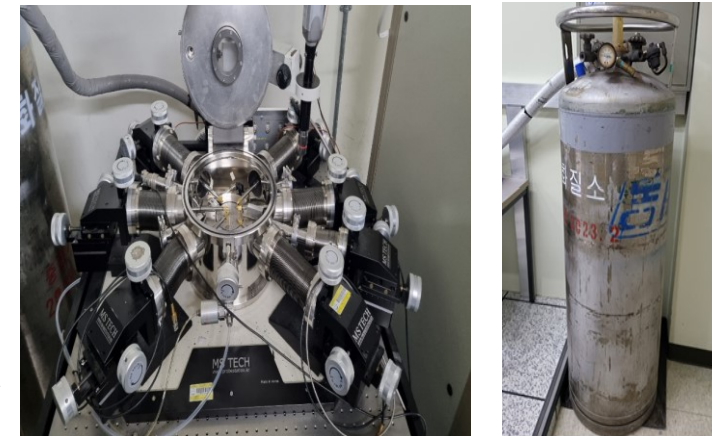
- Comprehensive analysis of DRAM at cryogenic temperature



- Fowler-Nordheim Stress degradation fo Buried-Channel-Array Transistors in DRAM Cell



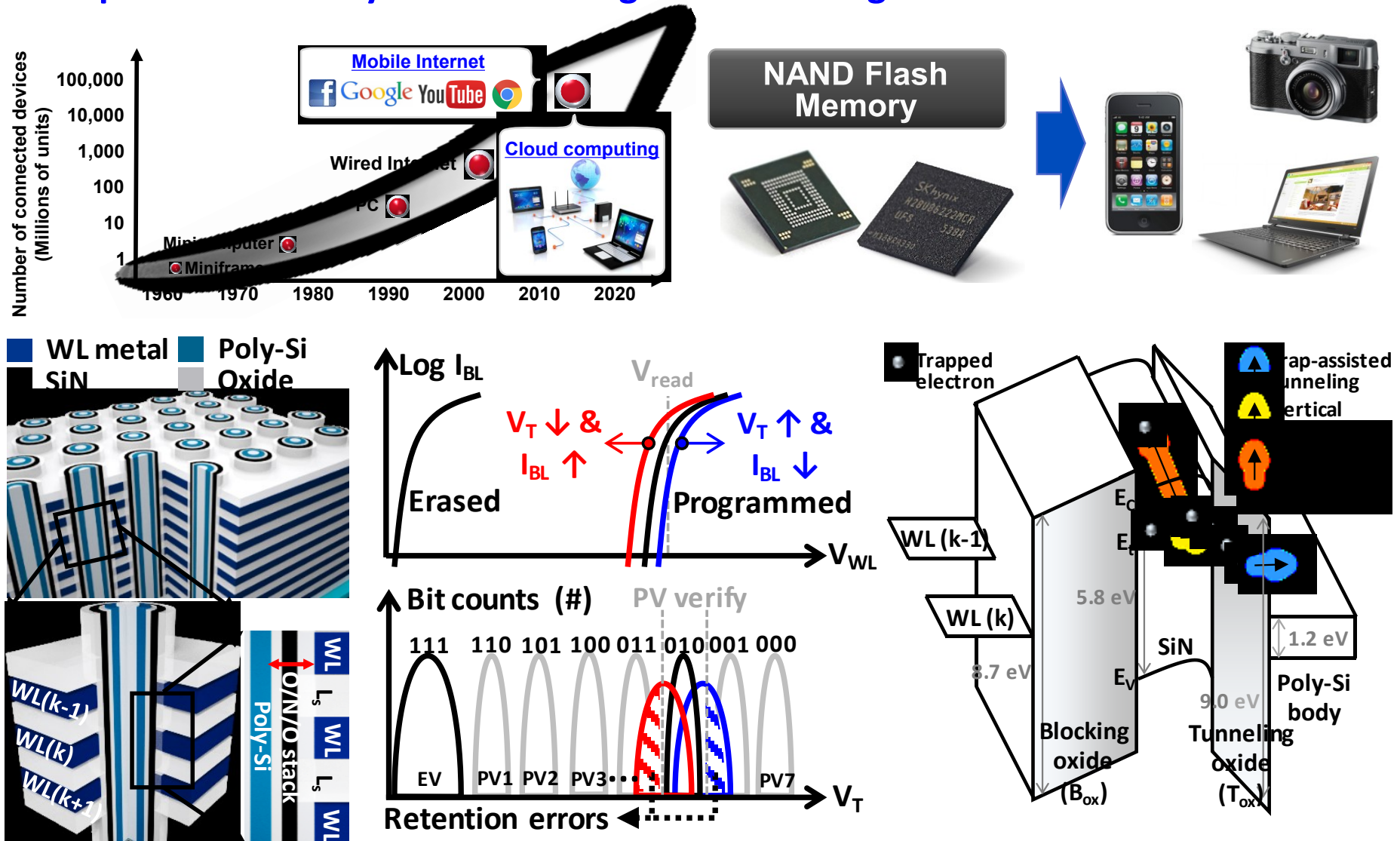
Vaccum chamber probe Station & Liquid Nitrogen



- Investigation of dynamic negative bias temperature instability DRAM peri transistors

# Memory: 3D NAND Flash Memory

- Comprehensive analysis of fast charge loss resulting from short time retention





The diagram illustrates the 3D XPoint memory architecture. It features a 3D grid of memory cells, each represented by a small cube. The cells are arranged in a 3x3x3 stack. The top layer of cells is highlighted in blue. The middle layer is highlighted in orange. The bottom layer is highlighted in green. The cells are connected by a network of perpendicular wires. The wires are color-coded: blue for the top layer, orange for the middle layer, and green for the bottom layer. The wires are arranged in a grid pattern, with each wire connecting to a specific cell in the stack. The diagram is set against a dark blue background.

**Cross Point Structure**  
Perpendicular wires connect submicroscopic columns. An individual memory cell can be addressed by selecting its top and bottom wire.

**Non-Volatile**  
3D XPoint™ Technology is non-volatile—which means your data doesn't go away when your power goes away—making it a great choice for storage.

**High Endurance**  
Unlike other storage memory technologies, 3D XPoint™ Technology is not significantly impacted by the number of write cycles it can endure, making it more durable.

**Stackable**  
These thin layers of memory can be stacked on top of each other.

**Selector**  
Whereas DRAM requires a transistor at each memory cell—making it big and expensive—the amount of voltage sent to each 3D XPoint™ Technology selector enables its memory cell to be written to or read without requiring a transistor.

**Memory Cell**  
Each memory cell can store a single bit of data.

Source : Western

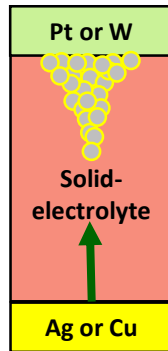


Figure 1 consists of three panels. The top-left panel is a schematic diagram of the device structure, showing a stack of layers: Column Line, Top Electrode, Buffer Layer, PCM, Buffer Layer, Buffer Layer, OTS Buffer Layer, Bottom Electrode, and CA. The top-right panel is a TEM image showing the device structure with dimensions: 72 nm for the TE layer, 104 nm for the PCM layer, 20 nm for the buffer layer, and labels for OTS, buffer, and BE layers. The bottom panel is a phase transition diagram showing Temperature vs. Time. It illustrates the RESET pulse (red) and SET pulse (blue) cycles, with the Read operation (black) occurring at a low current. The diagram also shows the phase transition between the Crystalline Phase and the Amorphous Phase, with the transition temperature  $T_{melt}$  and  $T_{cry}$  indicated.

Figure 1 consists of three panels. Panel (a) is a TEM image showing the cross-section of the Mo/α-IGZO/FE HZO/TiN/Si stack. Panel (b) shows XRD patterns for As Dep. (black line) and RTA (red line) samples. Panel (c) shows a schematic of the device and a table of parameters.

**(a) TEM Image:** The image shows a cross-section of the device stack. The layers are labeled from top to bottom: Mo, α-IGZO, FE HZO, TiN, and Si. A scale bar of 20 nm is shown in the bottom left corner.

**(b) XRD Patterns:** The plot shows Intensity (a.u.) versus  $2\theta$  (degree). The legend indicates two samples: As Dep. (black line) and RTA (red line). The peaks are labeled: o(111), t(101), o(200), t(110), and TiN. The RTA sample shows a sharp peak at  $2\theta \approx 31^\circ$  corresponding to the o(111) plane, while the As Dep. sample shows a broad peak at the same position.

**(c) Device & Ferroelectric parameters**

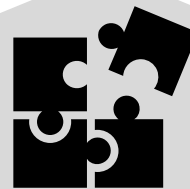
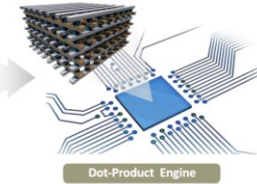
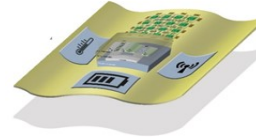
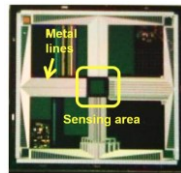
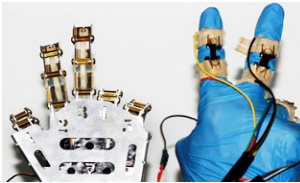
Gate Length	80 nm	Saturation Polarization ( $P_s$ )	40 $\mu\text{C}/\text{cm}^2$
S/D Doping Concentration	$10^{20}/\text{cm}^3$	Remanent Polarization ( $P_r$ )	20 $\mu\text{C}/\text{cm}^2$
Channel Concentration	$10^{18}/\text{cm}^3$	Coercive Field ( $E_c$ )	0.67 MV/cm
IL/FE Thickness	2/6.5 nm	Response time ( $\tau_r$ )	250 ns

The schematic diagram shows the device structure with Source (S), Drain (D), and Channel regions. The Gate is composed of HZO and IL layers. The inset shows the polarization vector  $P$  and the electric field vector  $E$  in the channel region.

# Application

## Smart IoT Devices & System

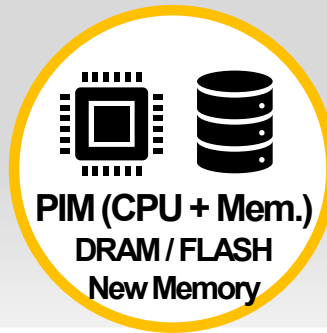
IoT Edge Devices + AI Processing → **Cognition and Response**



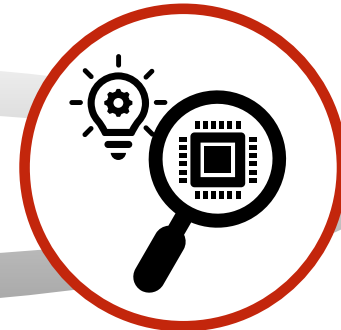
## Convergence



스마트 센서  
(케미컬, 바이오, 촉각)



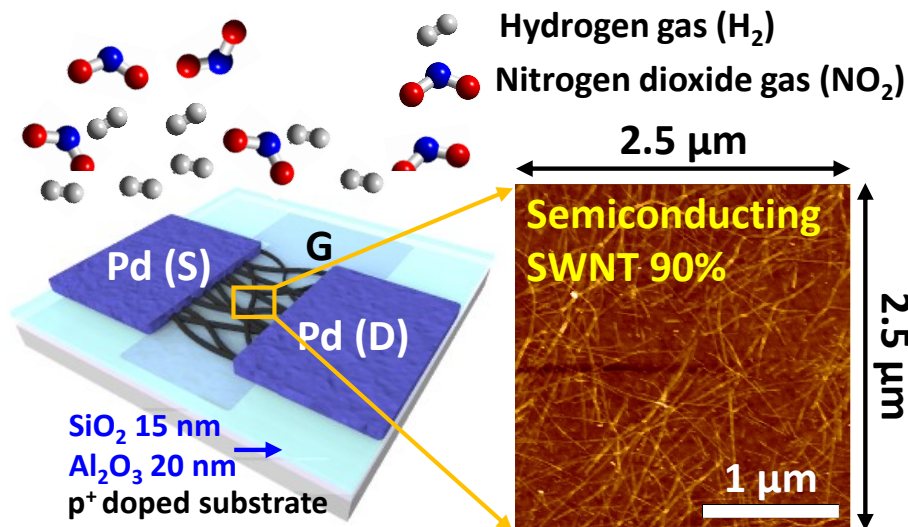
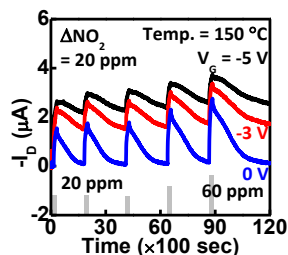
PIM (메모리 내 연산)  
지능형(AI) 반도체



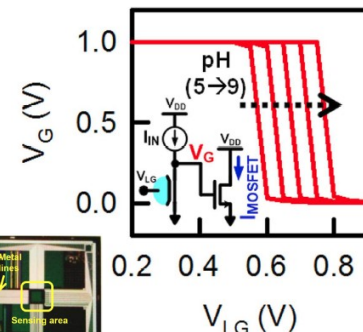
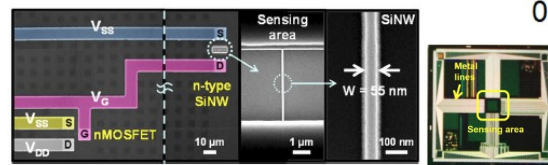
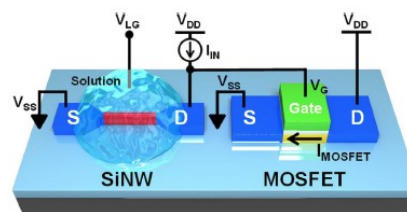
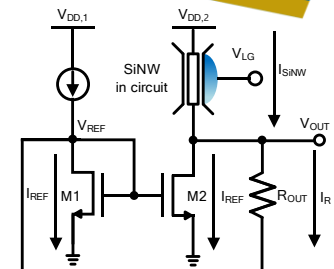
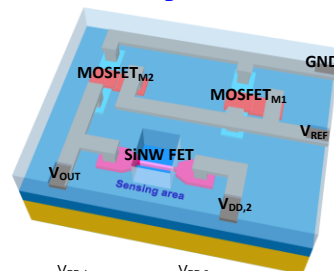
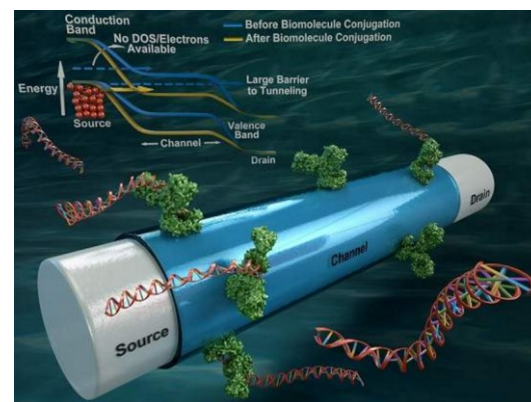
반도체 소자 기술  
(분석/최적화)  
(메모리/비메모리/디스플레이)

# FET-Based Chemical / Bio Sensors

## Gas Sensor



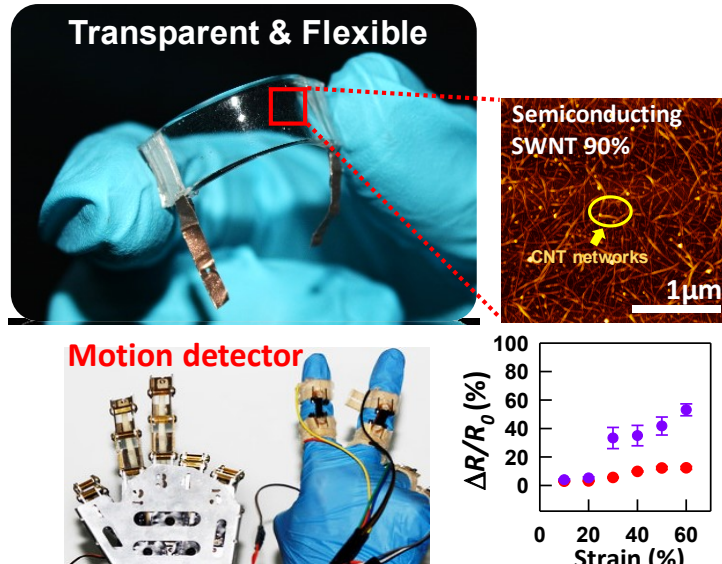
## Bio, pH Sensors & Circuitry



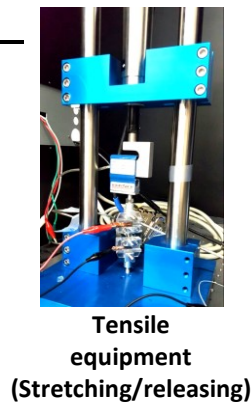
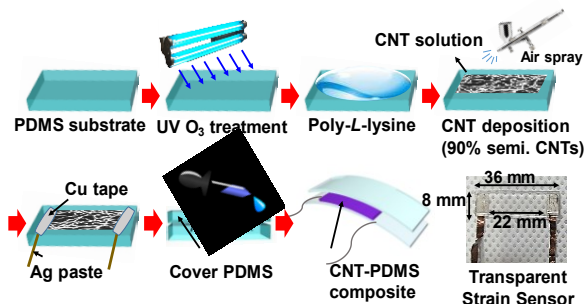


# Sensor: Strain / Pressure Sensors

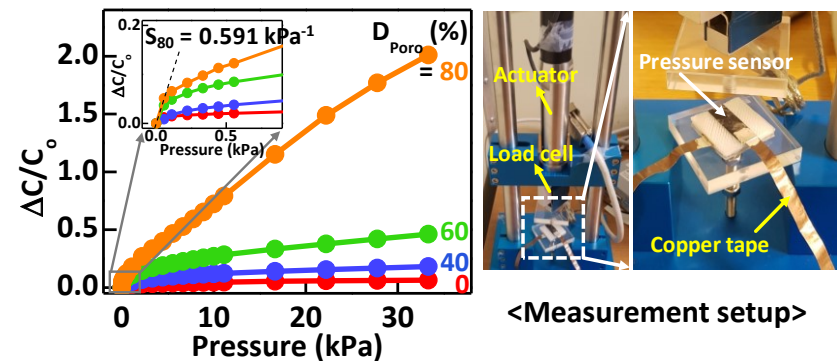
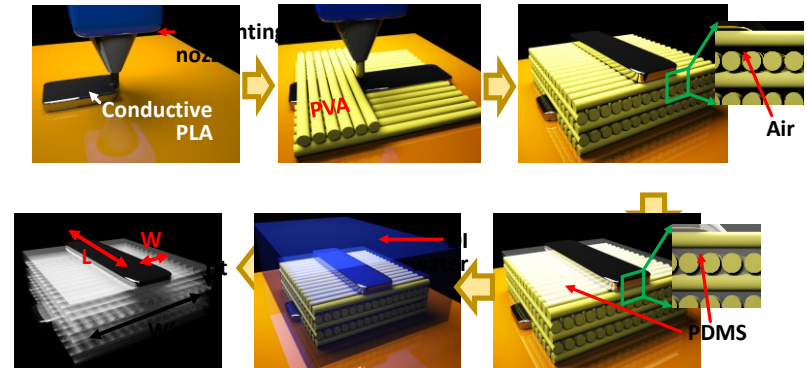
## CNT-PDMS strain sensor based on semiconducting SWNTs



## Fabrication process



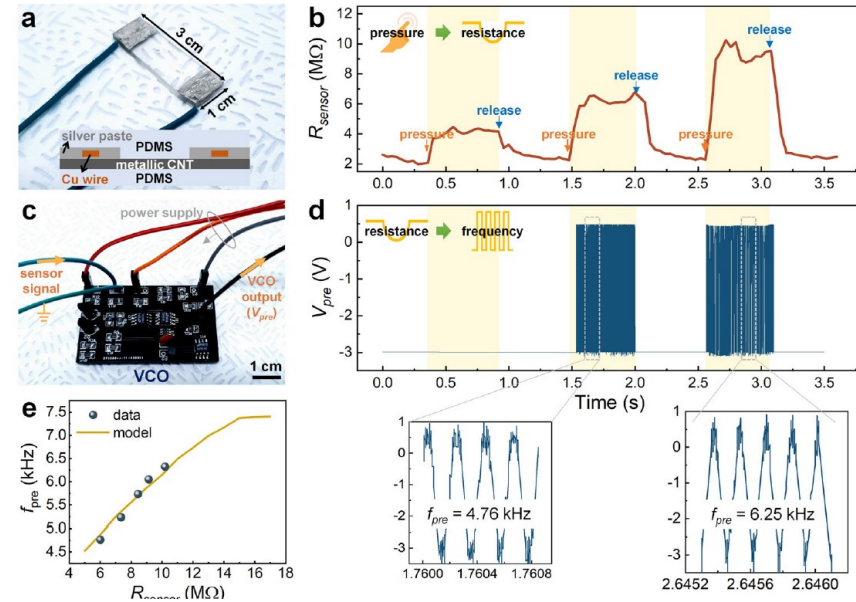
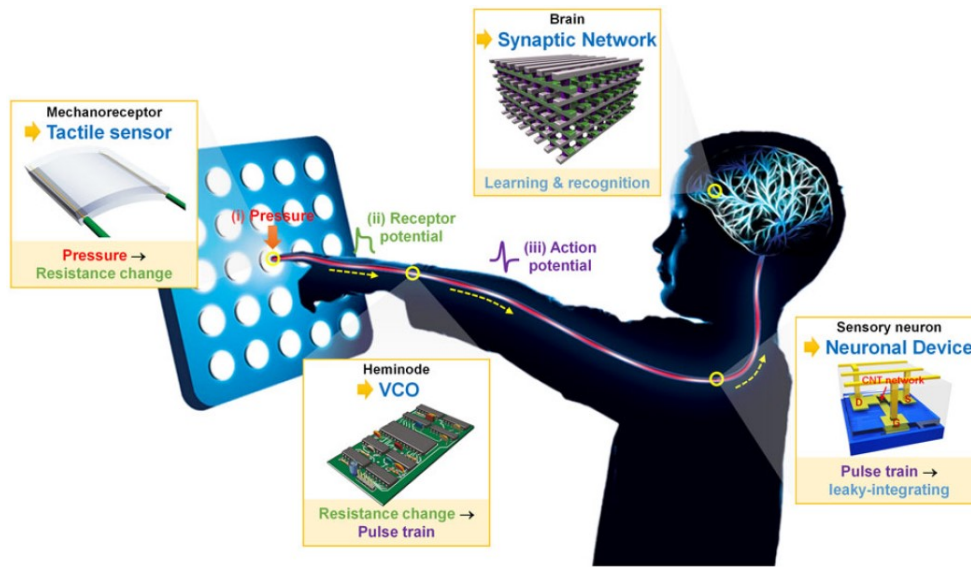
## 3D-printed pressure sensor with porous dielectric



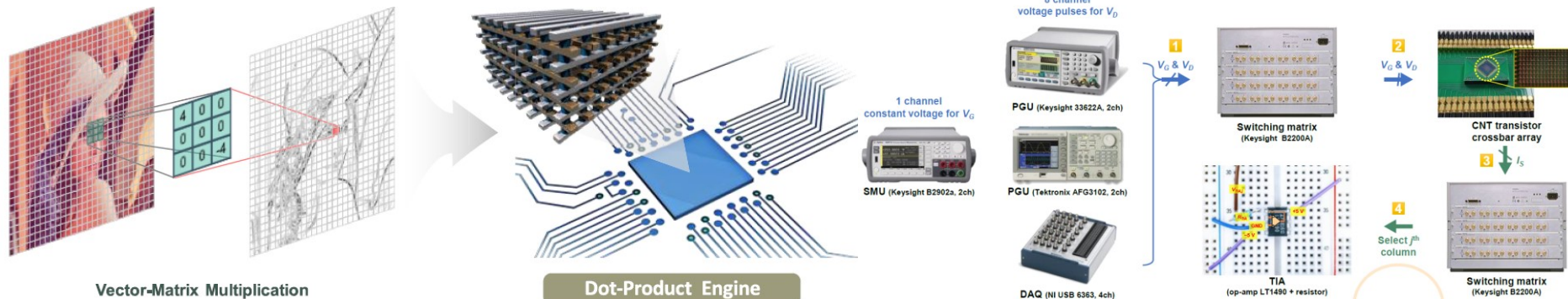


# Neuromorphic System (Intelligent Semicon.)

## Tactile Sensor System with sensory neurons and perceptual synaptic network

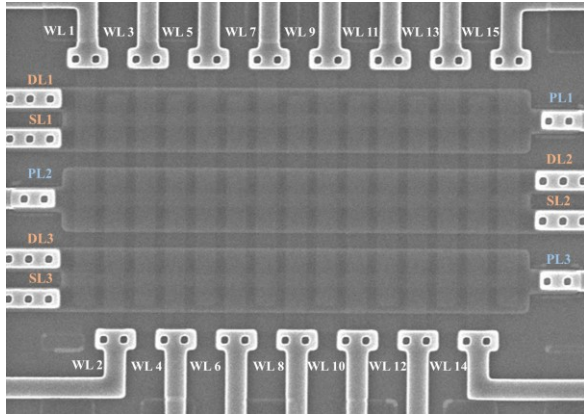


## Energy-efficient vector-matrix multiplication for in-memory computing



# Processing-In-Memory (PIM, Int. Semicon.)

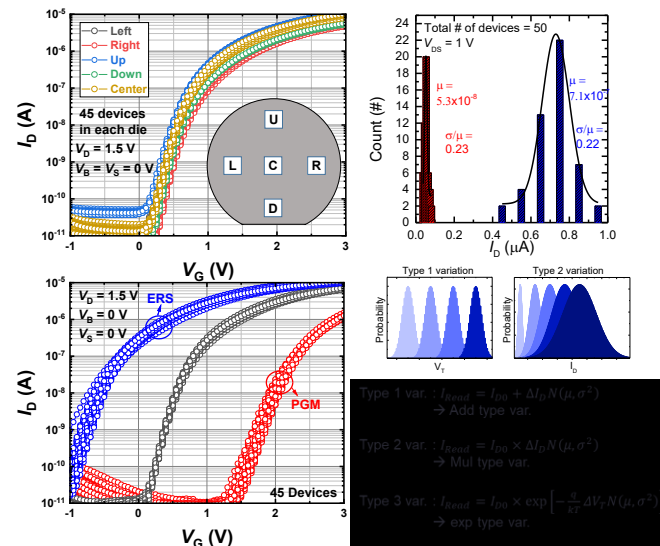
## FLASH Memory Array for PIM



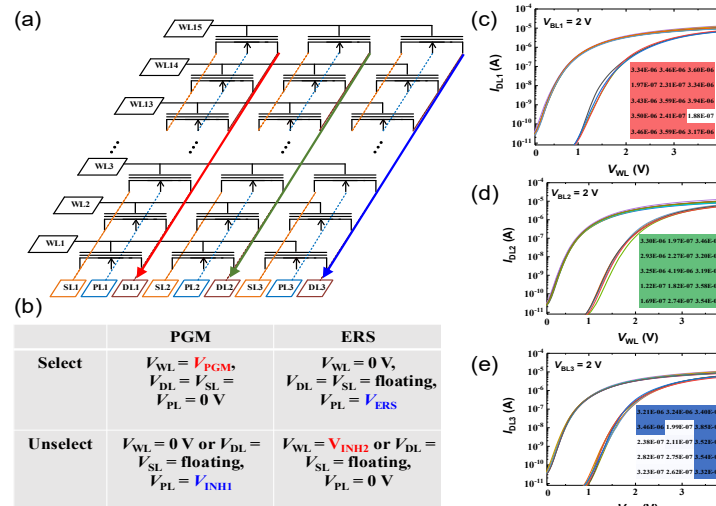
## Operating Principle (Architecture Design)

	PU	Mem.	PU	Mem.	PU
Role	Input	Weighting	Weighted sum	Activation function	Weighting
HW	Circuits	Memory Array	Capacitor + Circuits	Memory Array	Capacitor
Data form	$V_{in} \rightarrow V_{in} G t_{in} = Q \rightarrow \sum V_{in} G t_{in} = \Sigma Q \rightarrow V \rightarrow V_{in} \text{ or } t_{in} \rightarrow V_{in} G t_{in} \rightarrow \sum V_{in} G t_{in} = Q \rightarrow V$				
SW	$I$ layer: $a_1^{(l)}, a_2^{(l)}, a_3^{(l)}$ $I+1$ layer: $\sum_{i \in I} w_{i1}^{(l)} a_i^{(l)} \rightarrow f(s_1^{(l+1)}) = a_1^{(l+1)}$ $I+2$ layer: $\sum_{j \in (I+1)} w_{j1}^{(l+1)} a_j^{(l+1)}$				

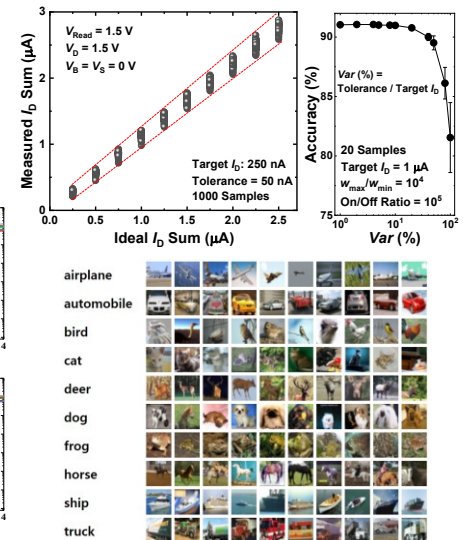
## FLASH Statistical Analysis



## Array Architecture Design for PIM

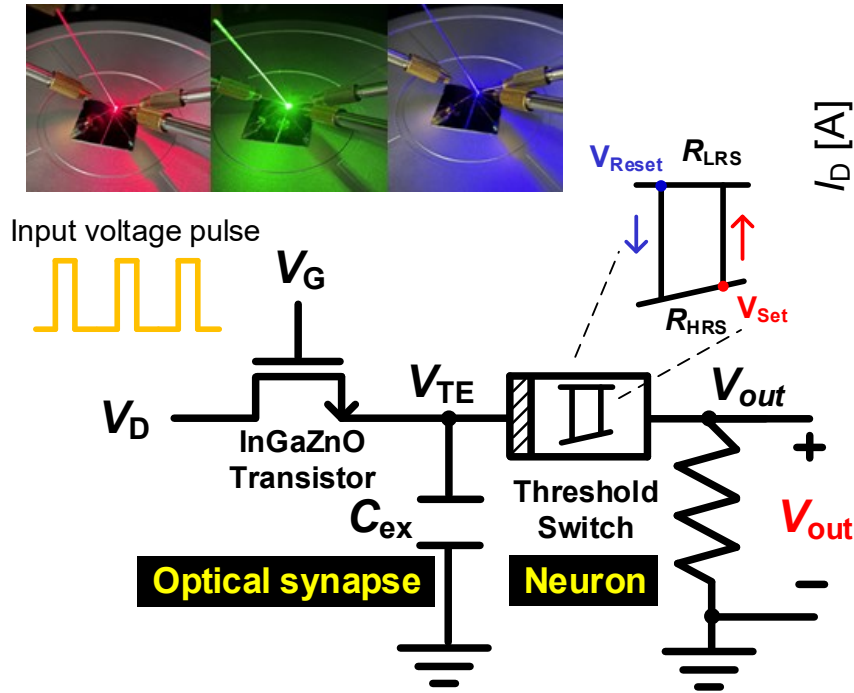


## Operating Accuracy

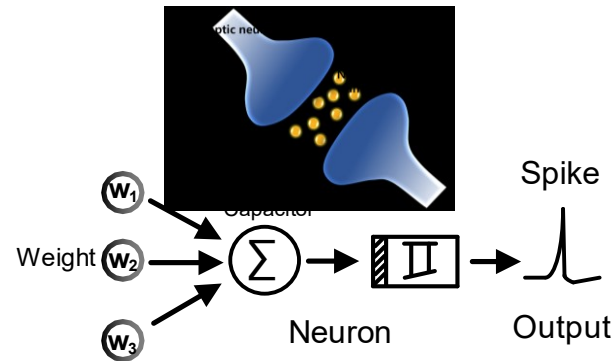
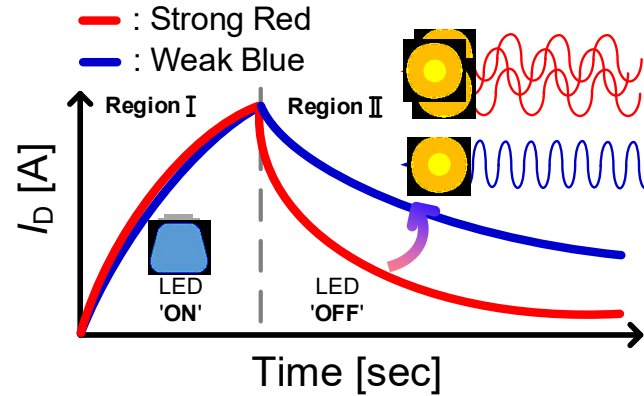


# Circadian Rhythm-Based Wearable Healthcare

## Leaky Integrate & Fire Neuron Circuit for Circadian Rhythm Diagnosis



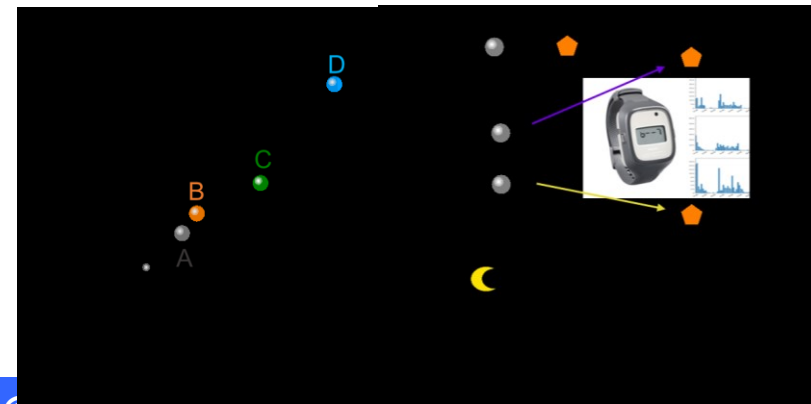
Spiking numbers with RGB light



Measuring HRV



Measuring EEG



# Summary

연구분야 : 반도체 기술 전반 (재료, 소자, 공정, 회로, 시스템)

응용분야 : 1) 상용 기술 개선 / 차세대 기술 개발 (메모리/비메모리)  
2) AI 반도체, 스마트 IoT 기기 및 스마트 시스템 개발  
(로직, 메모리, 디스플레이, 센서 etc.)

기술구분 :

- \* 소자 설계 (구조, 재료, 성능 확보 목표 (실용적 기술 지향))
- \* 공정 설계 (Process Design)
- \* 공정 기술/소자 제작 (Device Fabrication)
- \* 소자 분석 (측정, 분석, 시뮬레이션)
- \* 응용을 위한 반도체 회로 및 시스템

산학협력 (반도체전공트랙 참여기관) :

- \* SAMSUNG, LG, (주)Alsemy, (주)써카디언, 등. (확대 계획)