2022 반도체전공트랙 간담회

지능형 반도체 소자 및 집적회로 연구실
(*i*-S!LK)

School of Electrical Engineering,
Kookmin University

지도교수: 김대환, 최성진, 배종호, 김동명

Professor

Prof. Dong Myong Kim, Ph.D.

- ✓ Seoul National University, BSEE, (1986. 2.)
- ✓ Seoul National University, MSEE, (1988. 2.)
- ✓ University of Minnesota (Government scholarship), Ph.D.EE, (1993. 2.)
- ✓ Korea Institute of Science and Technology(KIST), Researcher, (1988. 2. - 1989. 8.)
- ✓ School of Electrical Eng., Kookmin Univ., Professor, (1993. 3. ~)

Prof. Sung-Jin Choi, Ph.D.

- ✓ Chung-Ang University, BSEE, (2007. 2.)
- ✓ KAIST, MSEE, (2008. 8.)
- ✓ KAIST, Ph.D.EE, (2012. 2.)
- ✓ ETRI: Electronics and Telecommunications Research Institute, Assistant researcher (2009. 1 ~ 2011. 1)
- ✓ University of California, Berkeley (PI: Prof. Jeffrey Bokor), Postdoctoral researcher (2011. 12 ~ 2013. 2)
- ✓ School of Electrical Eng., Kookmin Univ., Associate Professor (2013. 2. ~)

Prof. Dae Hwan Kim, Ph.D.

- ✓ Seoul National University, BSEE, (1996. 2.)
- ✓ Seoul National University, MSEE, (1998. 2.)
- ✓ Seoul National University, Ph.D.EE, (2002. 2.)
- ✓ Semiconductor Materials and Device Laboratory(SMDL) in Seoul National University, Postdoctoral researcher, (2002. 3. - 2002. 8.)
- ✓ Samsung Electronics, DRAM Design Team, Principal Research Engineer, (2002. 9. - 2005. 8.)
- ✓ University of Michigan, Ann Arbor,
- ✓ USA Visiting Scholar , (2012. 3. - 2013. 2.)
- ✓ School of Electrical Eng., Kookmin Univ., Professor (2005. 9. ~)

Prof. Jong-Ho Bae, Ph.D.

- ✓ Pohang University of Science and Technology, BSEE, (2011. 2.)
- ✓ Seoul National University, Ph.D.EE, (2018. 2.)
- ✓ Inter-university Semiconductor Research Center in Seoul National University, Assistant researcher, (2018. 3. - 2019. 7.)
- ✓ University of California, Berkeley (PI: Prof. Sayeef Salahuddin), Postdoctoral researcher (2019. 7 ~ 2020. 7)
- ✓ School of Electrical Eng., Kookmin Univ., Assistant Professor (2020. 9. ~)

Vision

다양한 연구 장려제도

- 삼성전자 · LG Display · SK Hynix 산학 협력을 통한 입사 추천!
- 등록금 지원
- 삼성전자 휴먼테크 논문대상 9회 (삼성전자 입사 특전)
- 박사과정 진학 권장 / 지원 (S!LK, 문부성 장학생, 미국유학 등)
- 연구과제 수행 - 졸업논문 주제의 연관성 최대한 확보
- 외국 대학 internship 제도 활용 지원

S!LK 졸업자 현황 (전체)

- 삼성전자/디스플레이 : 48명
- SK Hynix/SKC : 10명
- LG display/Innotek/SiliconWorks : 26명
- DB HiTek : 8명
- 외국기업(Intel / IBM / BOE) : 3명
- 대학/연구소 : 2명
- Magnachip/SEMES : 3명
- 기타 : 18명

교육 Plan

- 탄탄한 기초 이론
- 실용적인 실험/분석 능력 배양
- 반도체 소자 기초 이론에서부터, 최신 기술 수준까지 Cover

~22' S!LK 실적

SCI급 국제 저널 **407**편
특허 **72**건
국내/국외 학회 발표 **314**회
수상 **33**회

<최근 졸업생>
삼성전자 (9) LG Display (10)
SK Hynix (4) DB HiTek (4)
LX 세미콘 SEMES
S!LK 박사과정 진학 (4)

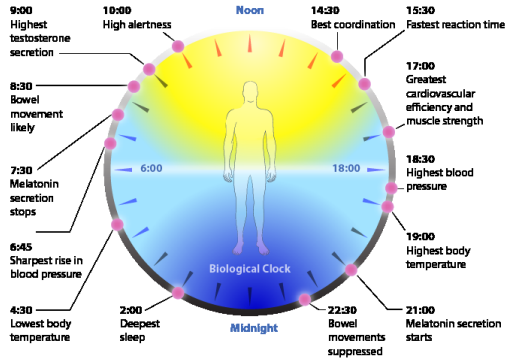
- 높은 취업률과 연구 성과 (평균 SCI(E) 논문 주저자 2.6편 + 공동저자 5.3편)
- 예비 석사 제도 – 석박사 진학 예정자 / 체계적인 교육 / 맞춤형 멘토–멘티 시스템

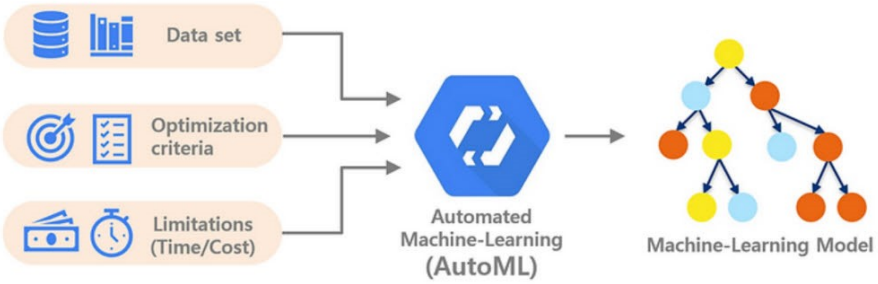
BK21 4단계, ERC(C-ICT 연구센터), 지능형반도체 관련 국책 과제 진행 중 (7개)

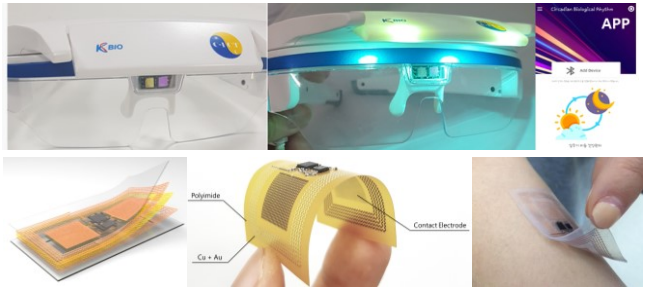
삼성전자/LG Display 외, 다양한 대/중소기업과 활발한 협업 (실용적 기술 지향)

Industry-University Co-op Project

반도체전공트랙 참여기업과의 산학협력 연구 (진행 중)







인공지능 기반 반도체 소자 모델링

→ 반도체 소자 측정/분석, 모델링
→ 반도체 모델링/EDA Tool 개발/개선 (Alsys 2.0)
→ 인공지능 모델 (AI 모델) 개발/개선

써카디언 리듬 조절을 위한 스마트 IoT시스템
(스마트 IoT 기기 및 스마트 홈 시스템)

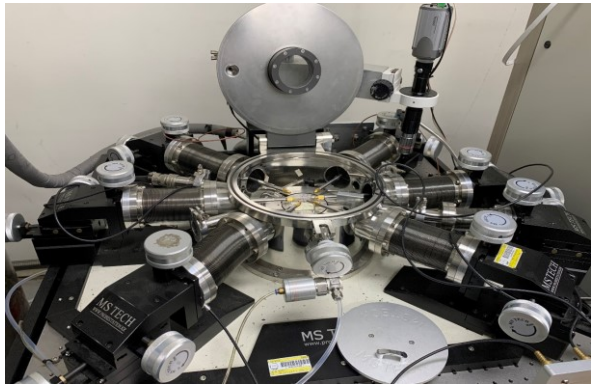
→ 지능형 반도체 설계 (소자/회로/시스템 수준)
→ 스마트 센서 설계 (소자/구동회로/시스템 수준)
→ 스마트 IoT 기기 및 시스템

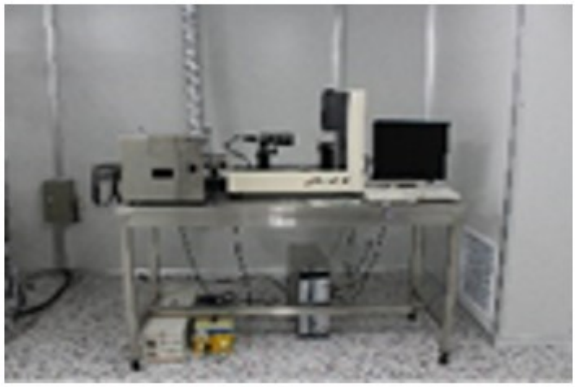
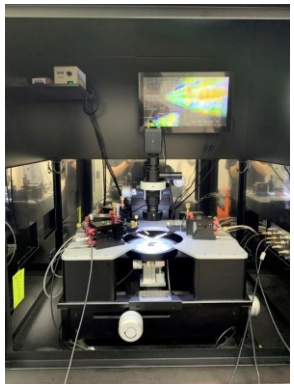
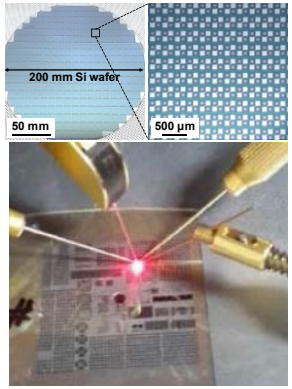
그 외 반도체전공트랙 참여기업으로
산학협력 프로젝트 확대 계획

→ 연구 경험 / 연구 참여 Chance!

Research Environment



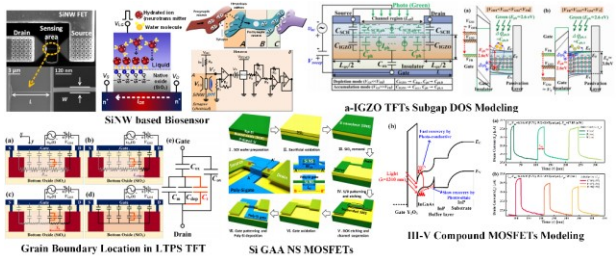


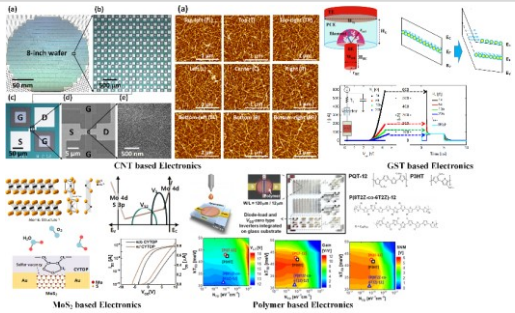
- 반도체 소자/회로 제작 (K-Fab. (클린룸), 산학협력관 5층)
- 측정/분석 시스템 구축
- 매 학기 self-user 교육 후 (대학원생), 직접 장비 사용의 기회

Research Field of S!LK

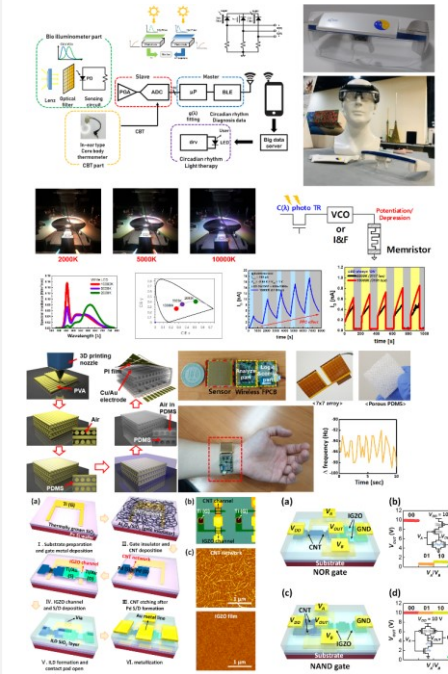
CMOS device and integrated circuits



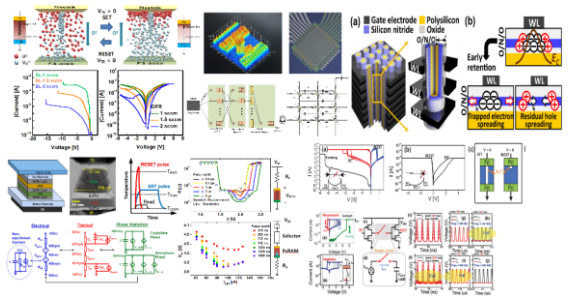
Emerging materials-based electronics



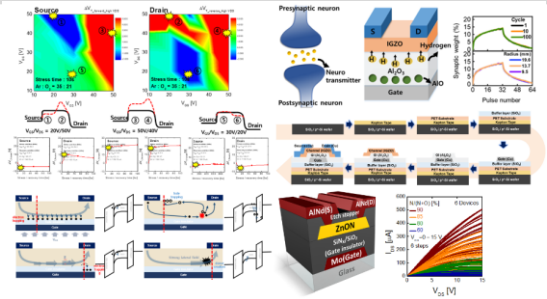
Hybrid device-based circadian ICT research center



Future Memory



Oxide materials-based electronics (Display)

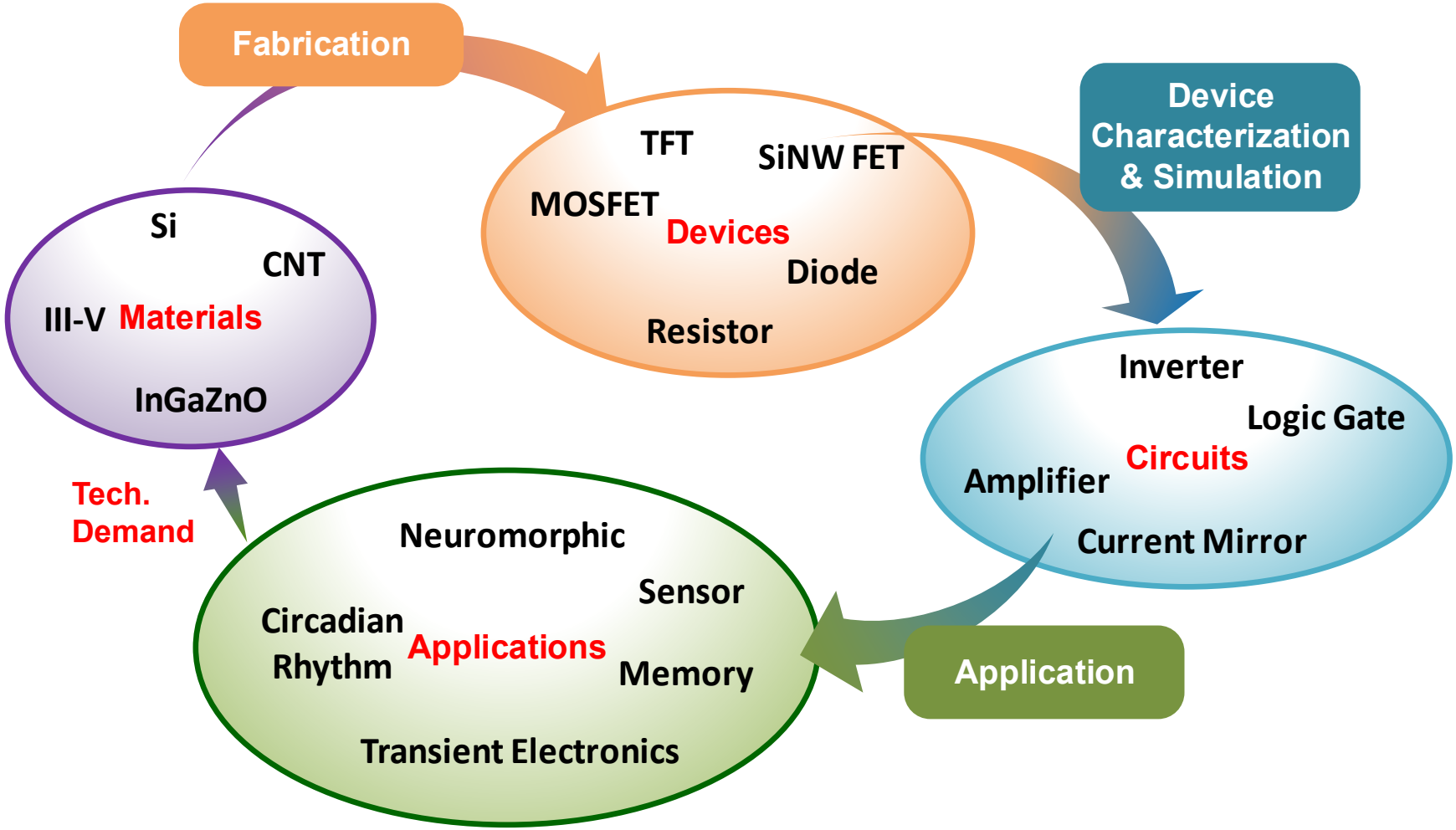


- 반도체 소자/회로/시스템 – 재료/구조/공정 설계/제작(공정) → 분석/모델링
- 반도체 응용 기술 연구 – 차세대 메모리/로직 반도체, 센서, 디스플레이, IoT 기기 등

반도체 재료/소자 구조 개발 → 분석/모델링 → (1) 새로운 응용 개발

→ (2) 개선점 발견 → 재료/소자 개발 (순환)

Research Direction of S!LK

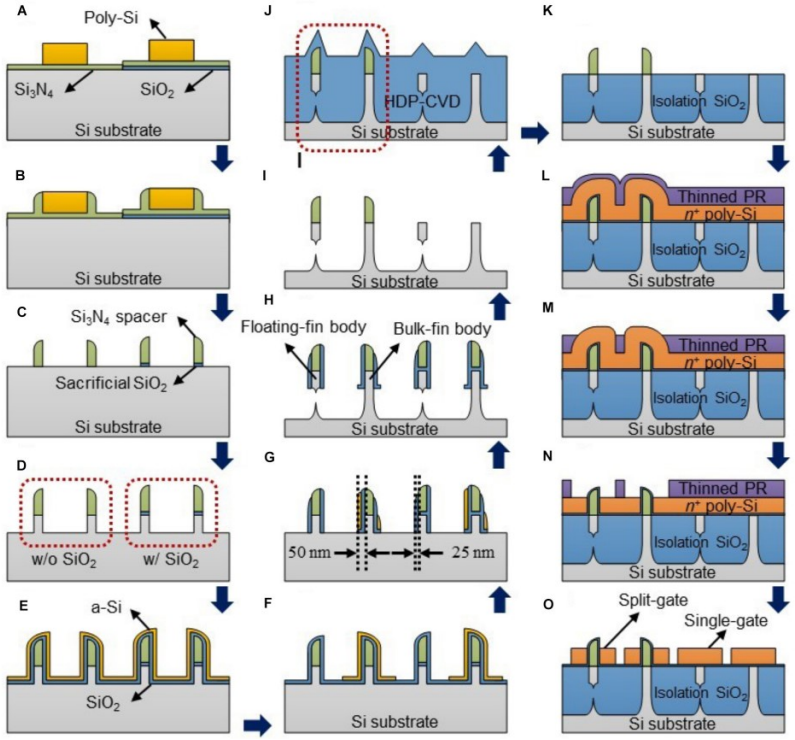


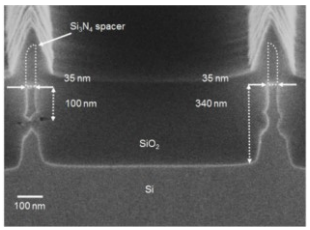
반도체 기본(재료, 이론, 공정) → 응용 (반도체 기술 전반)

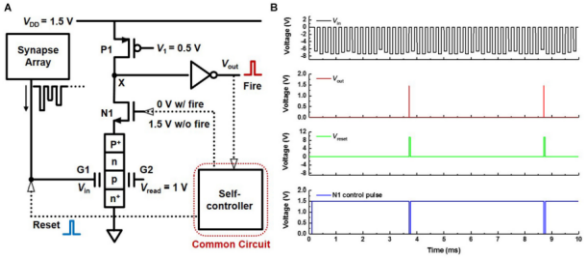
Device Fabrication

Device/CMOS Circuit Design & Fabrication, Process Design

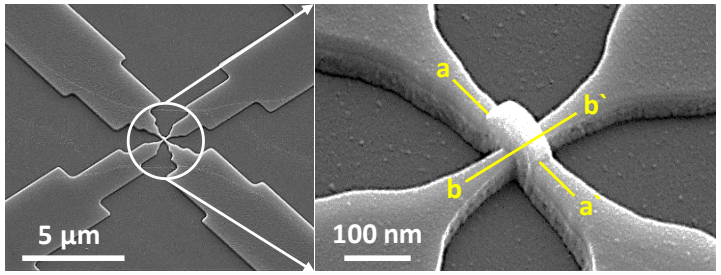
- **Fabrication Process Design (공정 설계/제작)**
  'New Device'–CMOS Circuit Cointegration

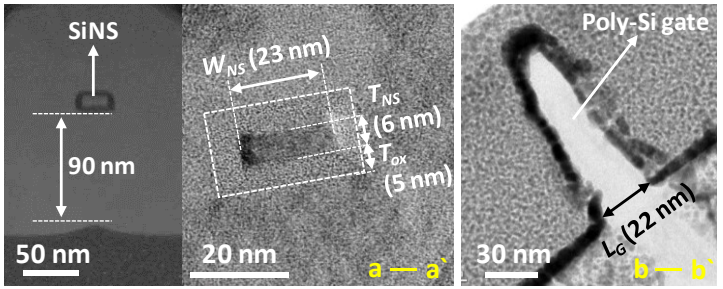




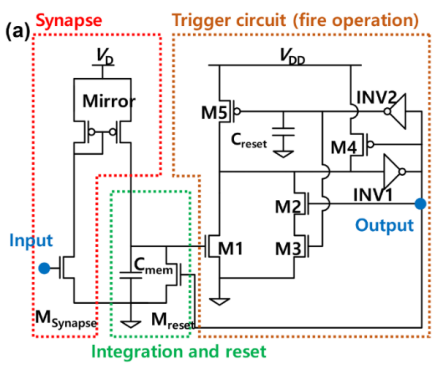


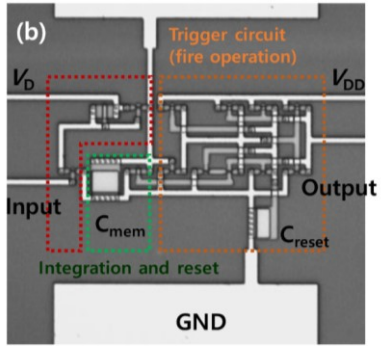
- **GAAFET (NNFC)**





- **Si CMOS Circuits for AI (ISRC)**
  (Processing-In-Memory, PIM)

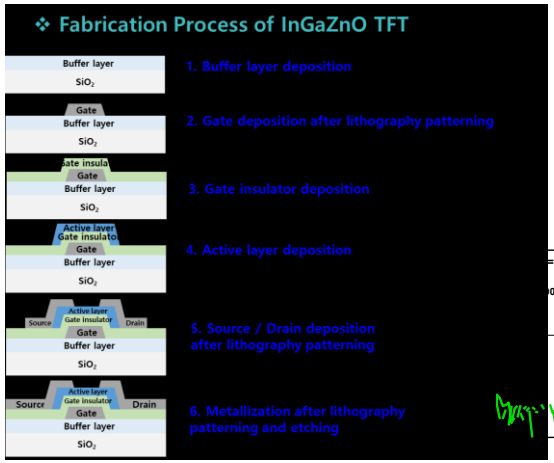


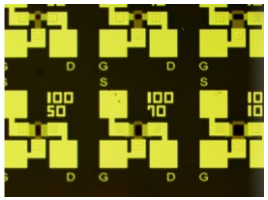


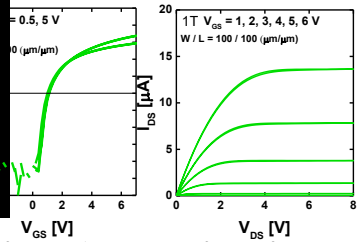
Device Fabrication in K-Fab.

(Display, Memory)

➢ IGZO TFT Fabrication







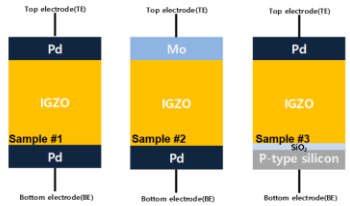
➢ ReRAM, Memristor Array Fabrication

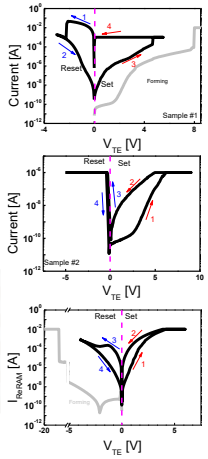
❖ **Pd/IGZO/Pd, Mo/IGZO/Pd**

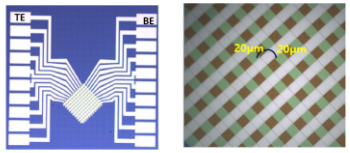
- SiO_2 (300 nm) oxidation wafer
- Bottom electrode deposition
  - → E-beam evaporator(Ti : 2nm , Pd : 40 nm)
- IGZO deposition
  - → Sputter(Ar : O_2 = 3 : 2sccm, RF power = 150W, ≅ 60nm)
- Top electrode deposition
  - → E-beam evaporator(Ti : 2nm, Pd : 40 nm) : Sample #1
  - → E-beam evaporator(Ti : 2nm, Mo : 40 nm) : Sample #2

❖ **Pd/IGZO/p-type silicon**

- SiO_2 (300 nm) oxidation wafer
- Bottom electrode deposition
  - → E-beam evaporator(Ti : 2nm , Si : 40 nm)
- Annealing
  - → Oven(120°, 15min)
- IGZO deposition
  - → Sputter(Ar : O_2 = 3 : 2sccm, RF power = 150W, ≅ 60nm)
- Top electrode deposition
  - → E-beam evaporator(Ti : 2nm, Pd : 40 nm)

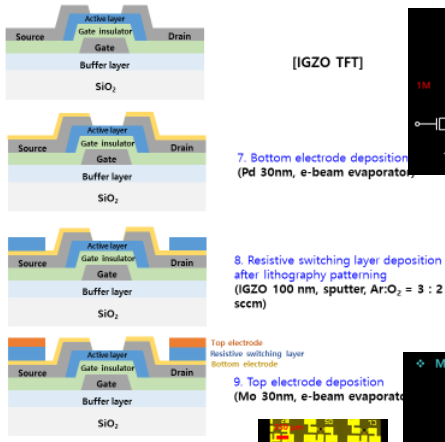


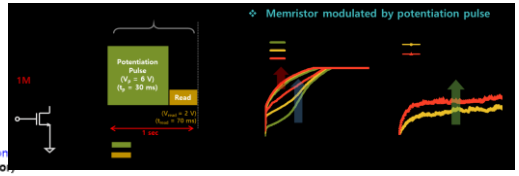


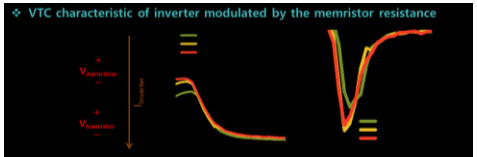


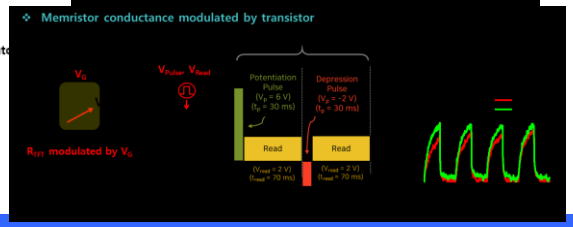
➢ 1T1M(1Transistor 1Memristor) Fabrication

❖ Fabrication Process of InGaZnO TFT and InGaZnO memristor

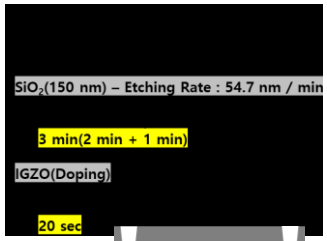


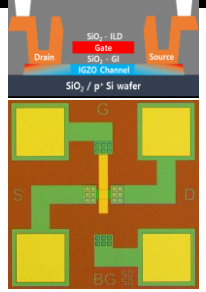


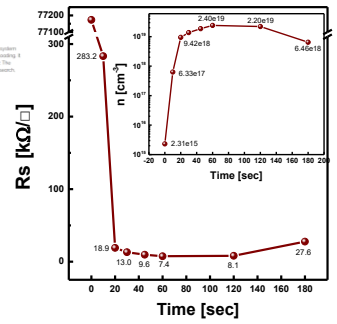


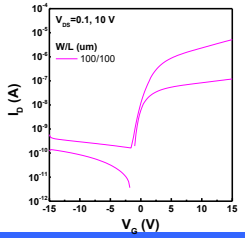


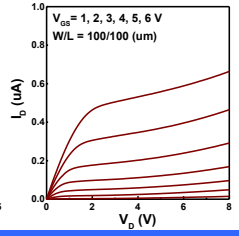
➢ IGZO TFT with Top Gate Self Aligned Coplanar Structure Fabrication.









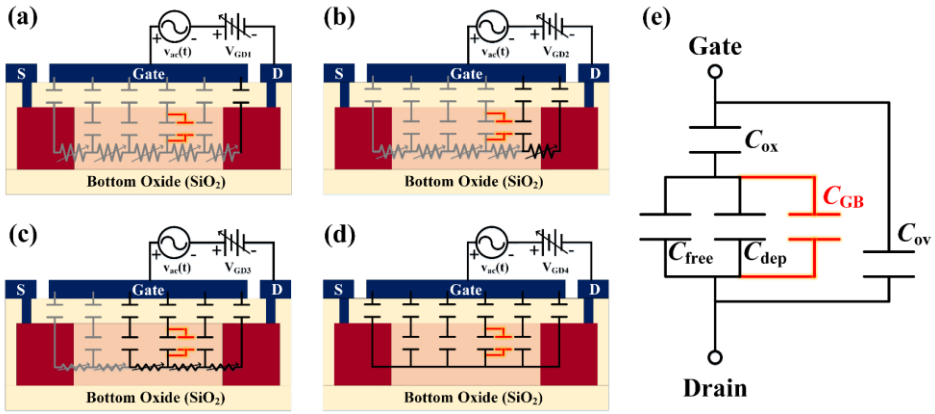


Device Modeling and Characterization

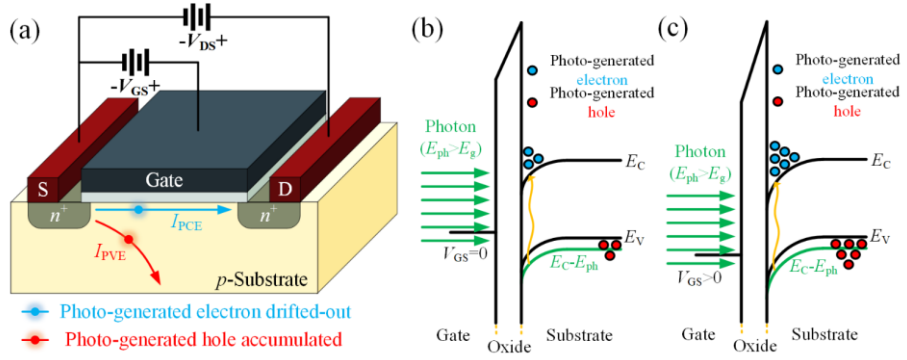
(Analysis on Generic Devices–Memory, Logic Tr., Display Tr., etc.)

❖ **Modeling and Characterization of CMOS device using opto-electronic characteristics.**

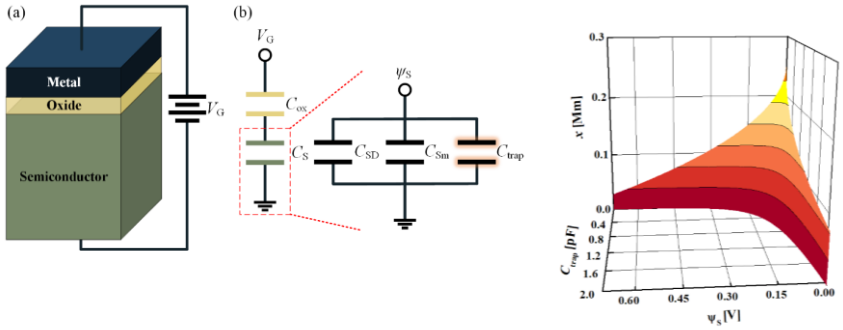
➢ Characterization of Grain Boundary Trap



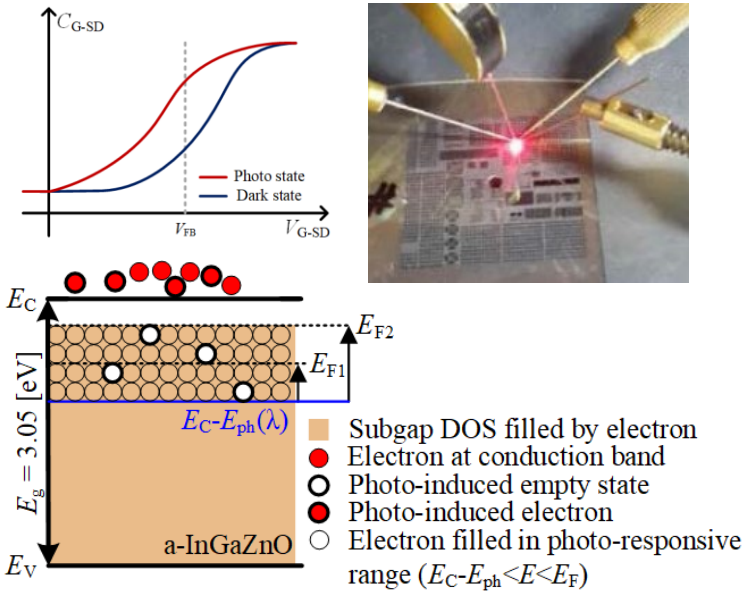
➢ Modeling of photonic response in MOSFETs



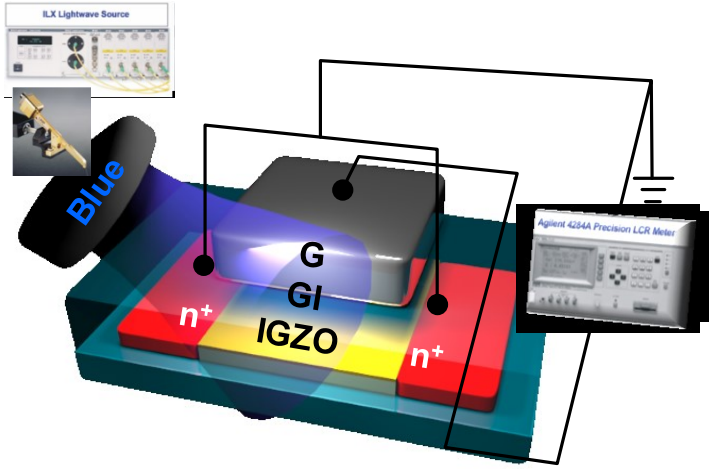
➢ Extraction of trap in MOS structure

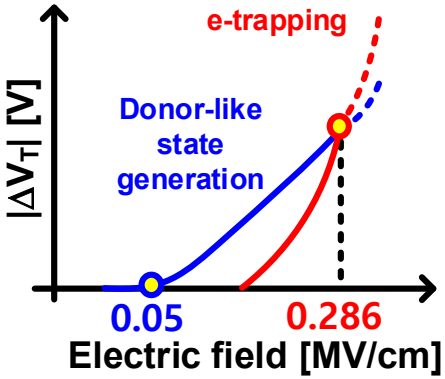


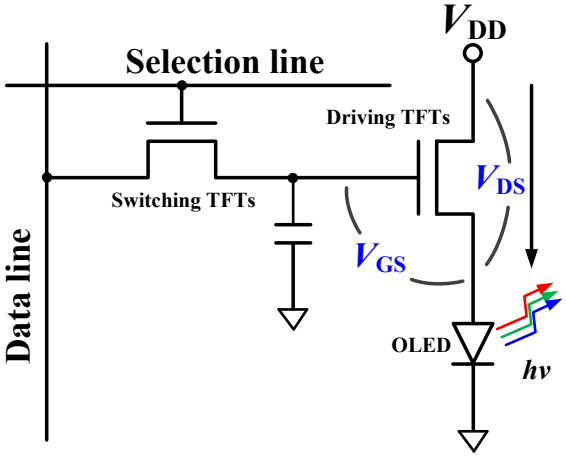
➢ Extraction of trap using opto-electronic technique

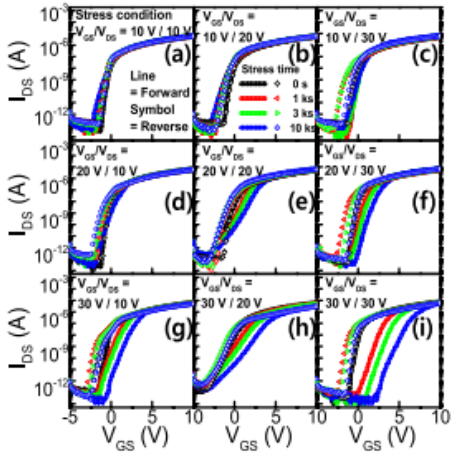


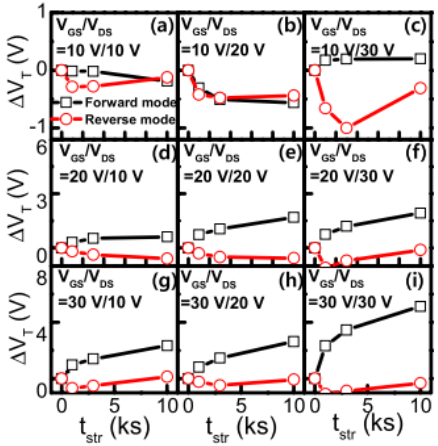
Device Modeling and Characterization
(Analysis on Display Devices)

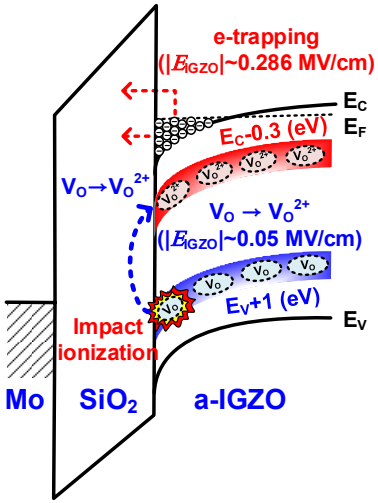






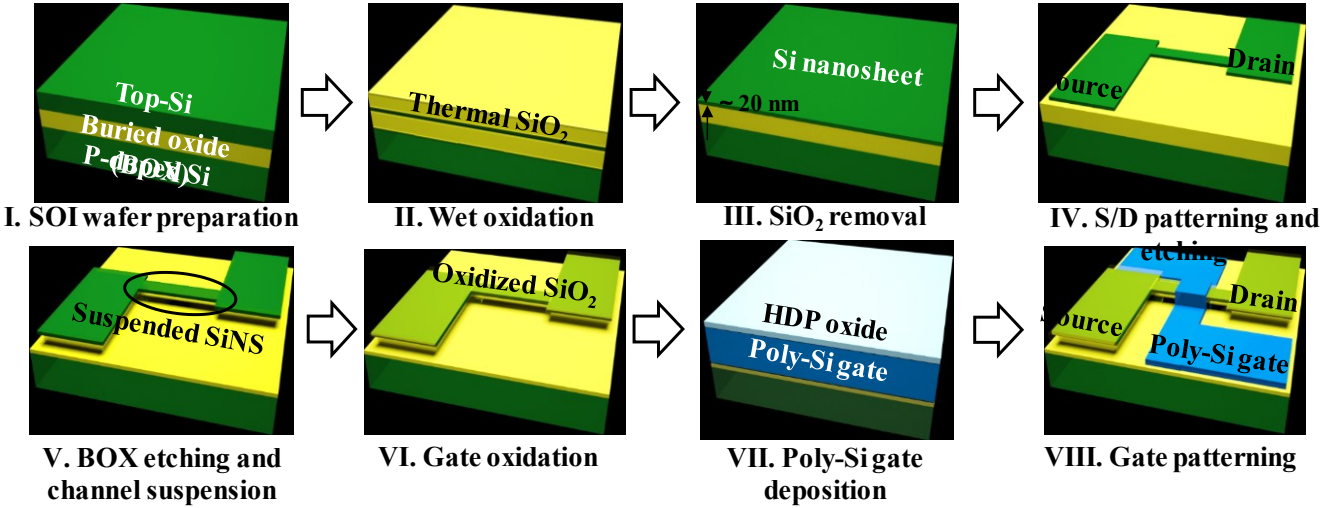


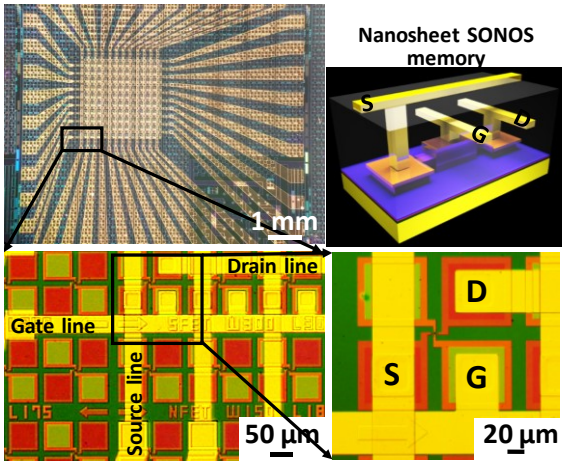


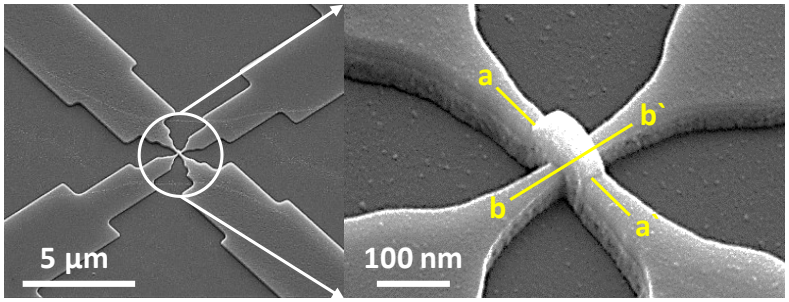


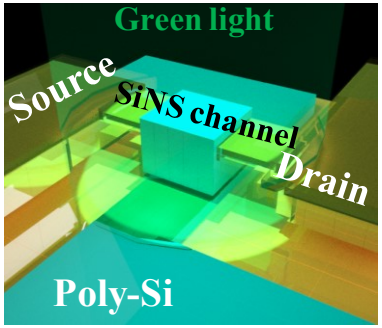
➔ **Transparent/Flexible Display**: Instability under OLED operation

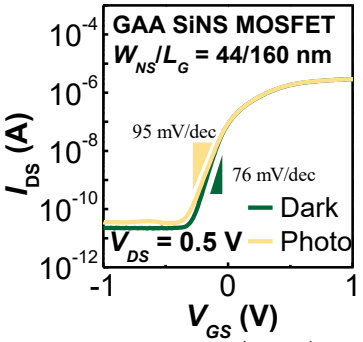
Logic: Gate-All-Around Si Nanosheet MOSFETs

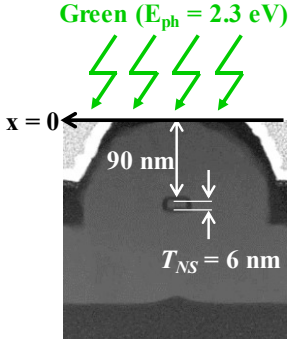


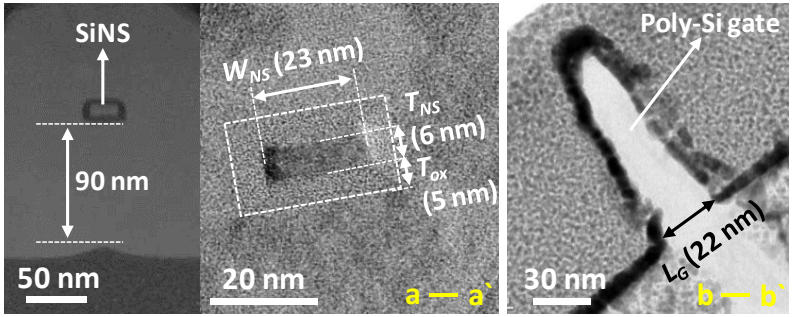










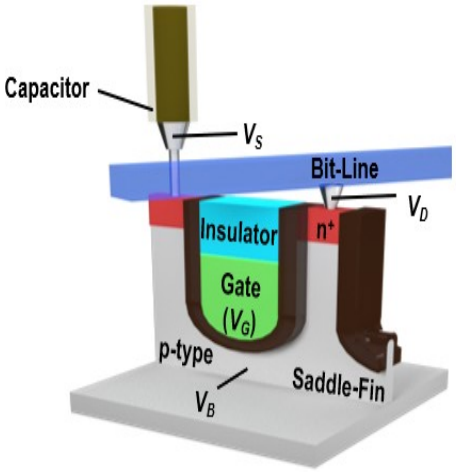


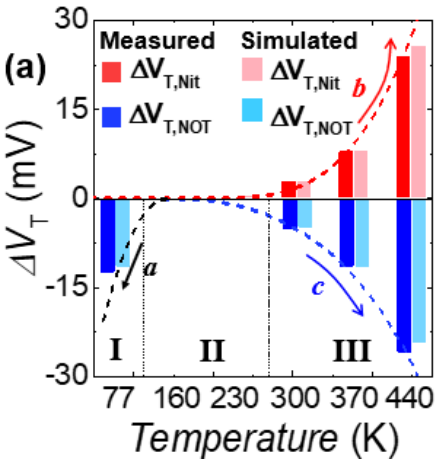
$$m_{photo} - m_{dark} = \Delta m(V_{GS}) = \frac{C_{photo}(V_{GS})}{C_{ox}}$$

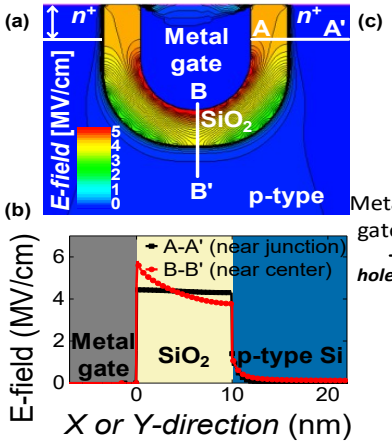
$$C_{photo}(\psi_s) = C_{ox} \int_{\psi_s(V_{GS})}^{\psi_s(V_{GS}+\Delta V_{GS})} \frac{d\Delta m(V_{GS})}{dV_{GS}} \cdot \left(\frac{d\psi_s}{dV_{GS}}\right)^{-1} d\psi_s$$

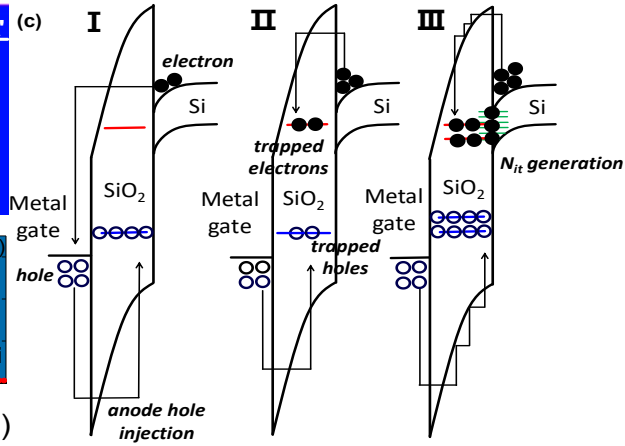
Memory: DRAM Cell TR, Peri TR

- **Comprehensive analysis of DRAM at cryogenic temperature**

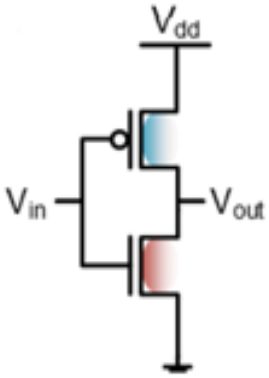


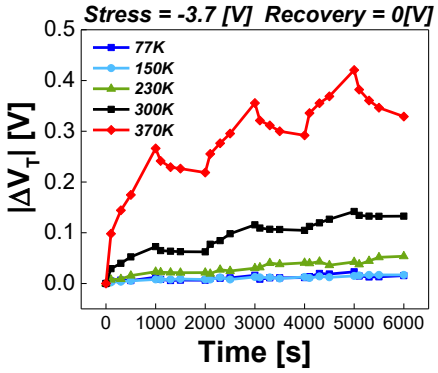


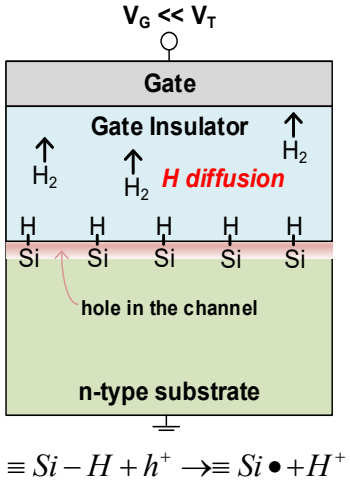




- **Fowler-Nordheim Stress degration fo Buried-Channel-Array Transistors in DRAM Cell**

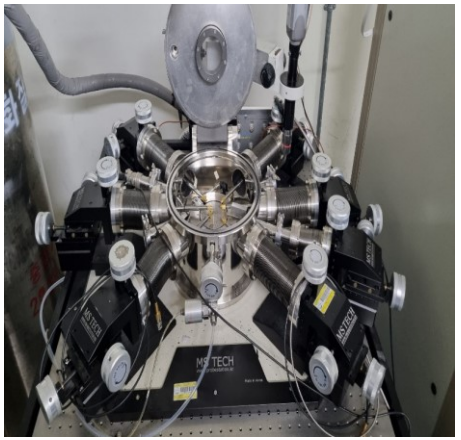






$$\equiv Si - H + h^+ \rightarrow \equiv Si\bullet + H^+$$

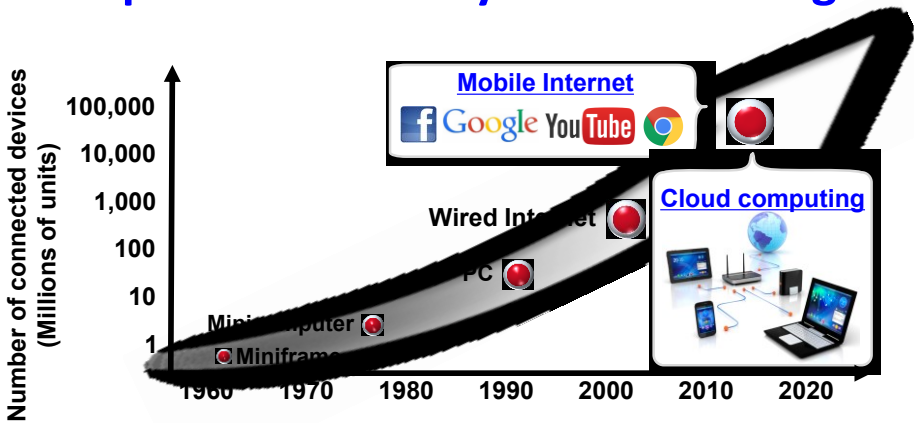
Vaccum chamber probe Station & Liquid Nitrogen

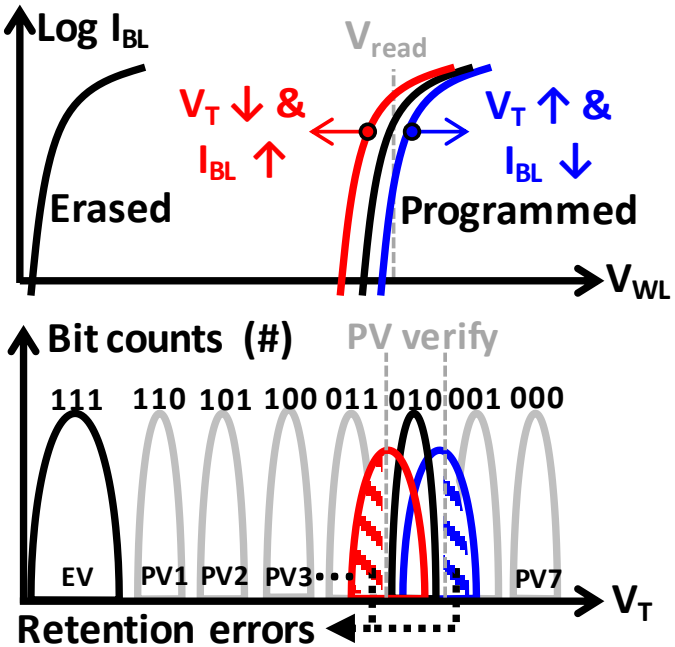


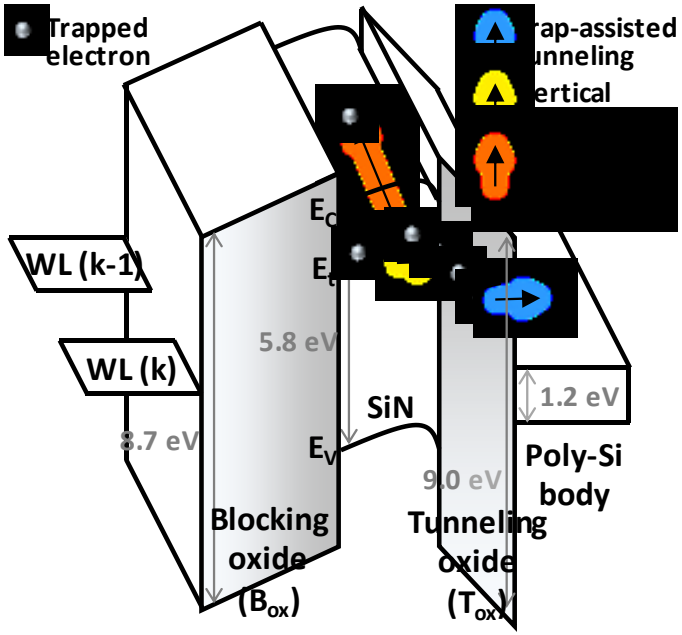
- **Investigation of dynamic negative bias temperature instability DRAM peri transistors**

Memory: 3D NAND Flash Memory

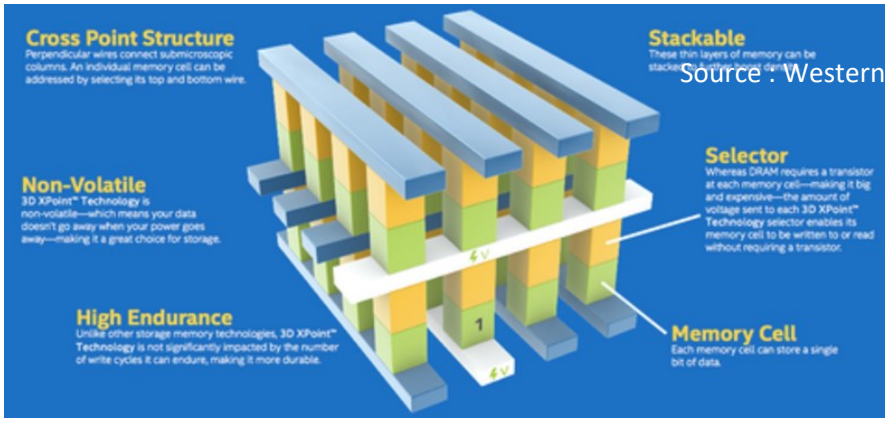
- Comprehensive analysis of fast charge loss resulting from short time retention





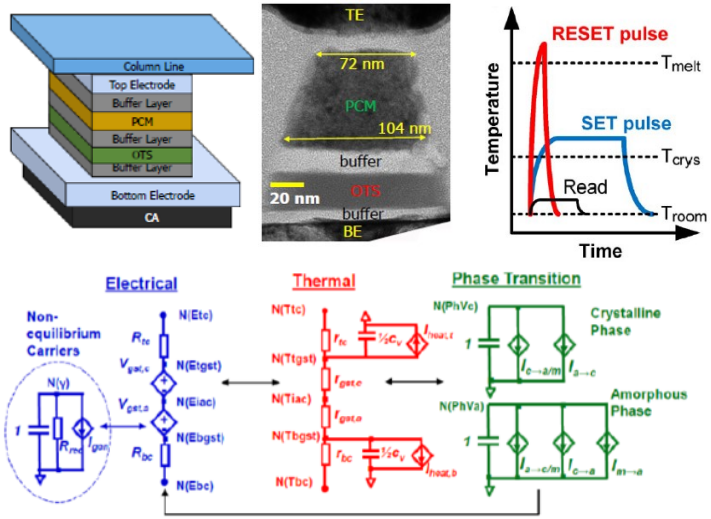


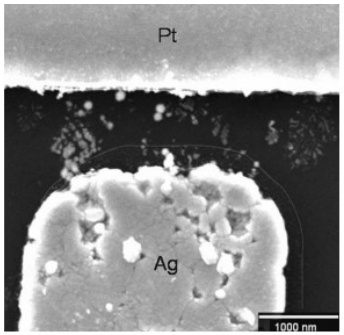
Memory: Emerging Memory

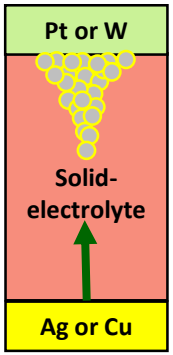


Source : Western

Phase-Change RAM

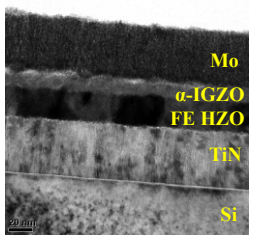


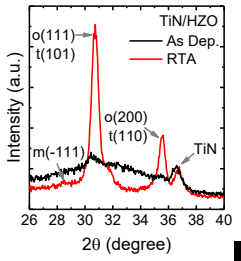


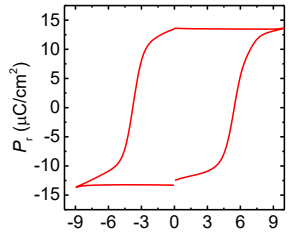


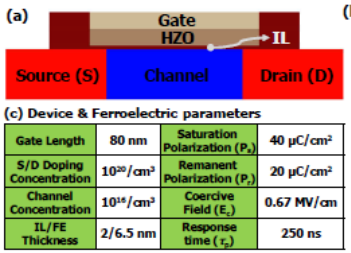
Conducting-Bridge RAM

Ferroelectric RAM



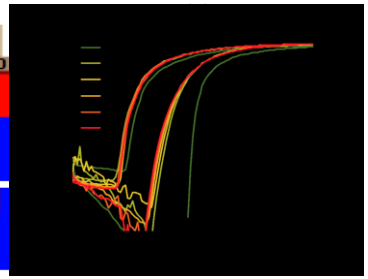


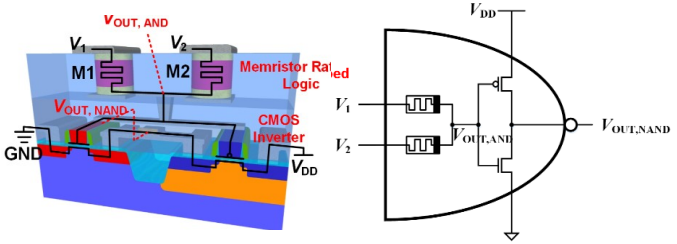


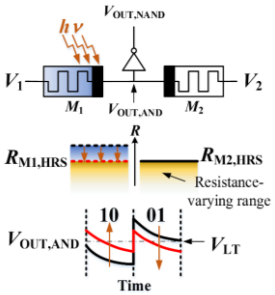


(c) Device & Ferroelectric parameters

Gate Length	80 nm	Saturation Polarization (P_s)	40 μC/cm²
S/D Doping Concentration	10^{20}/cm³	Remanent Polarization (P_r)	20 μC/cm²
Channel Concentration	10^{16}/cm³	Coercive Field (E_c)	0.67 MV/cm
IL/FE Thickness	2/6.5 nm	Response time (τ_p)	250 ns





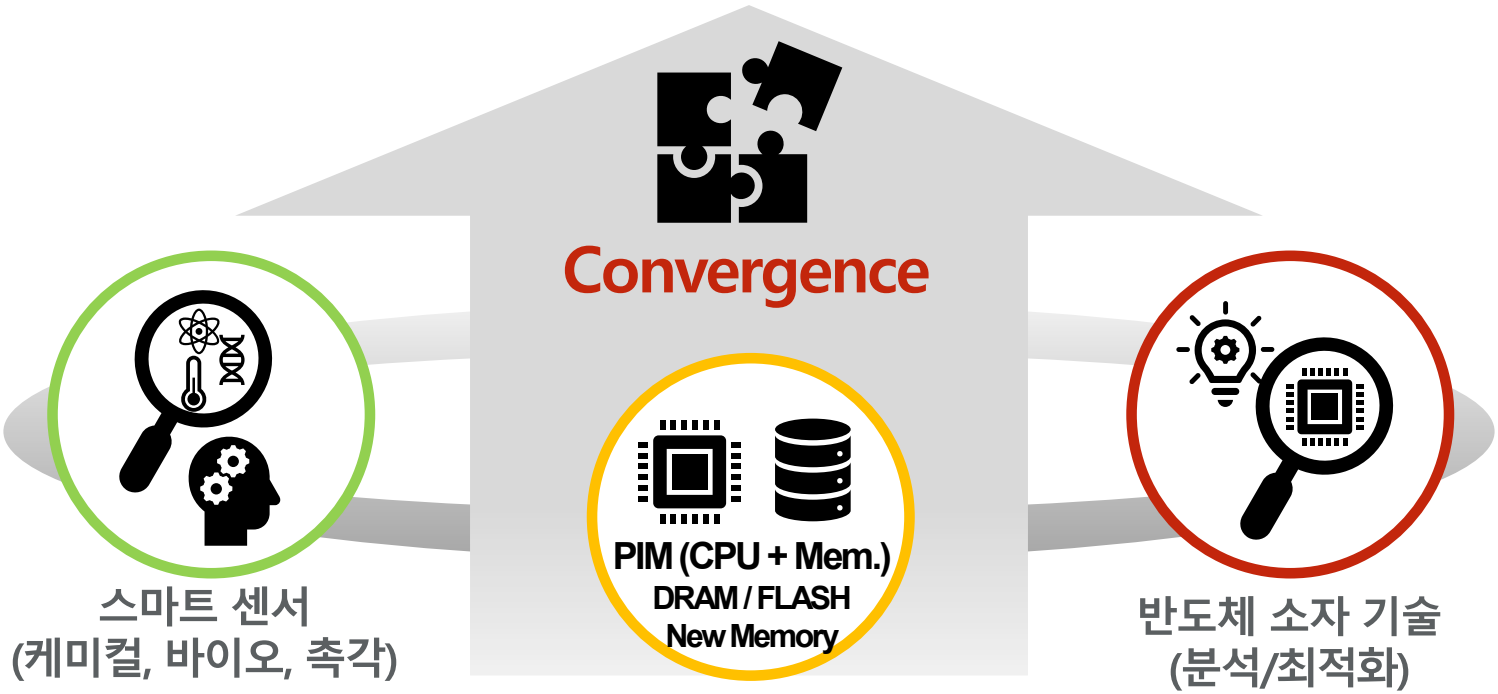


Memristor Ratioed Logic

Application

Smart IoT Devices & System

IoT Edge Devices + AI Processing → Cognition and Response



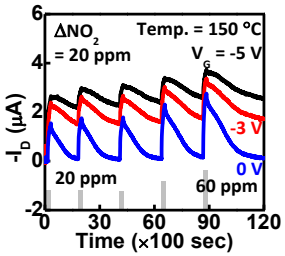
스마트 센서
(케미컬, 바이오, 촉각)

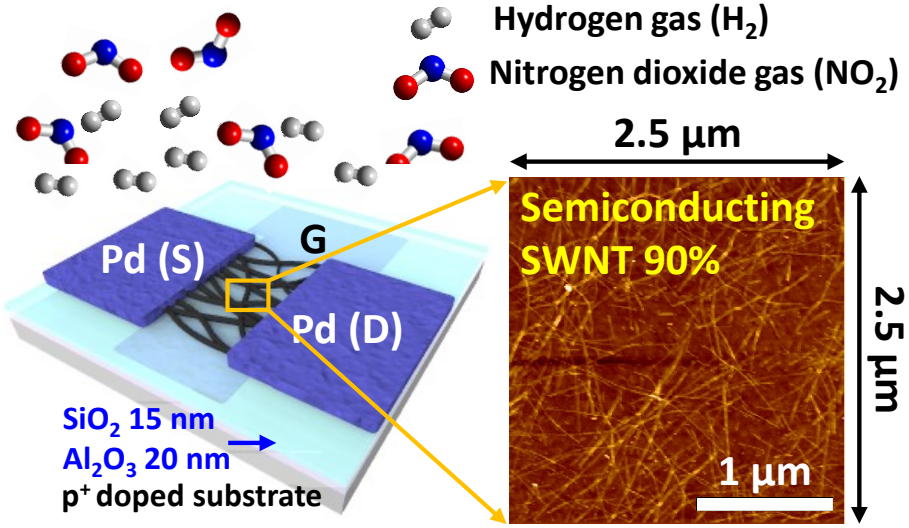
PIM (메모리 내 연산)
지능형(AI) 반도체

반도체 소자 기술
(분석/최적화)
(메모리/비메모리/디스플레이)

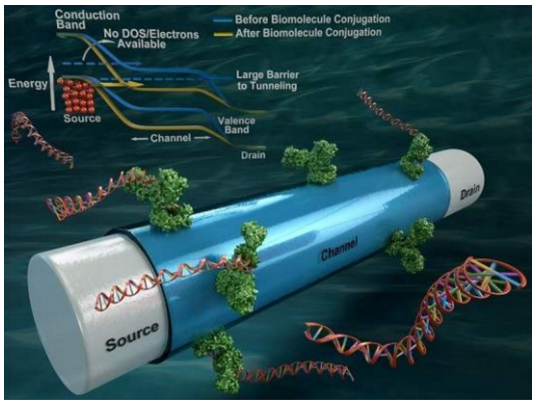
FET-Based Chemical / Bio Sensors

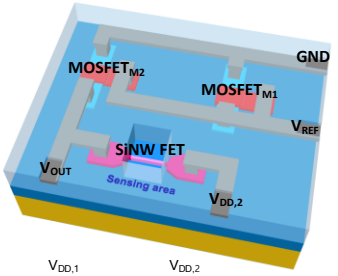
Gas Sensor

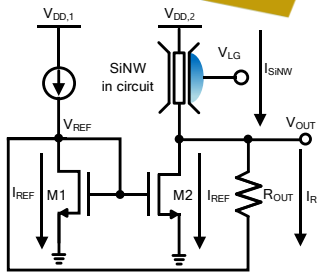


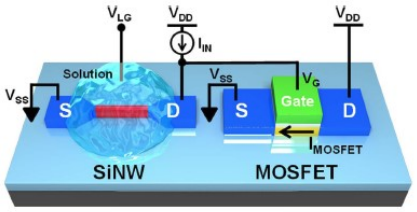


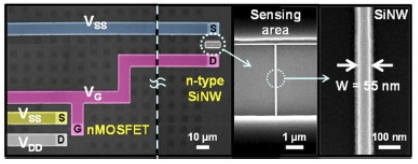
Bio, pH Sensors & Circuitry

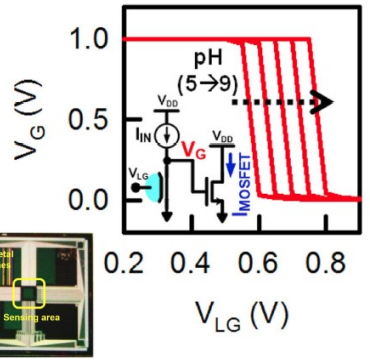






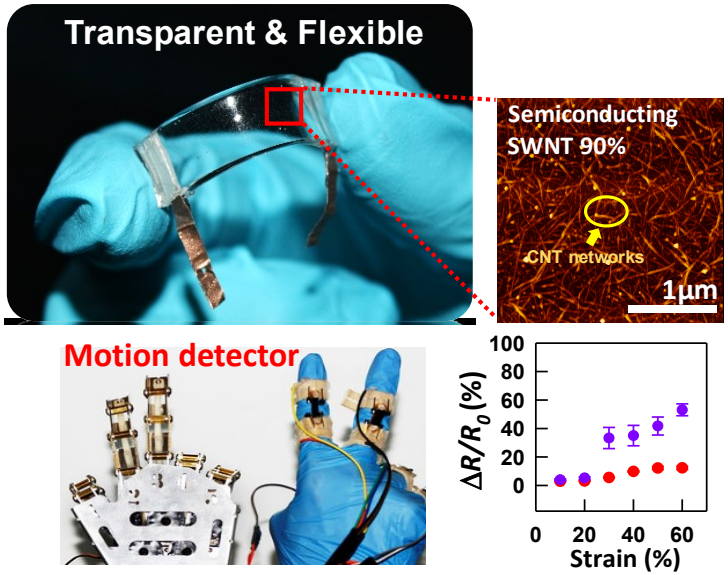




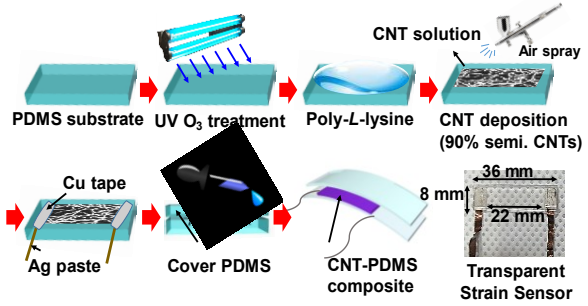


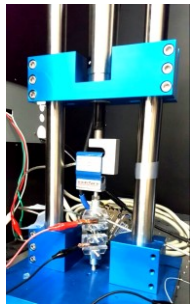
Sensor: Strain / Pressure Sensors

CNT-PDMS strain sensor based on semiconducting SWNTs



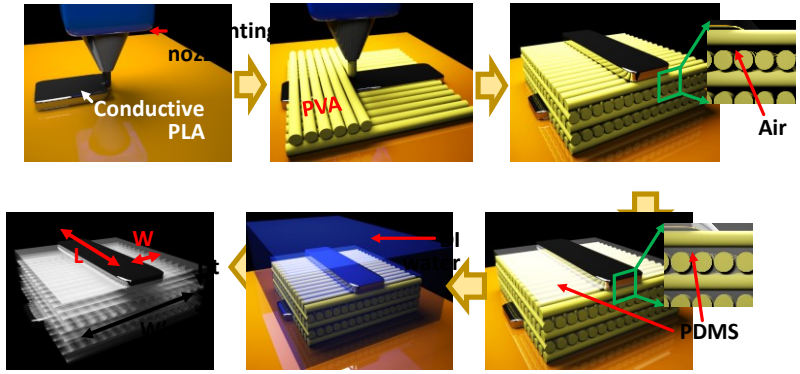
Fabrication process

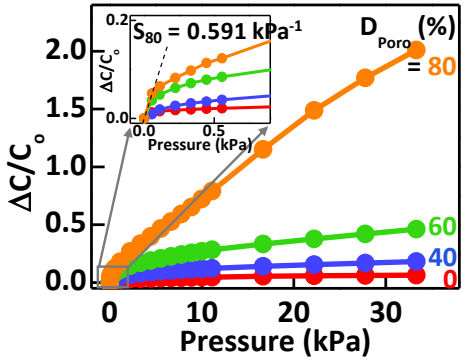


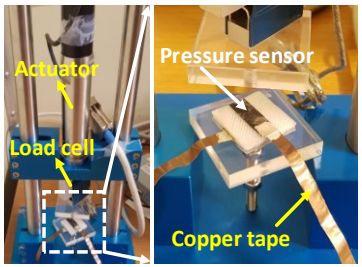


Tensile equipment (Stretching/releasing)

3D-printed pressure sensor with porous dielectric



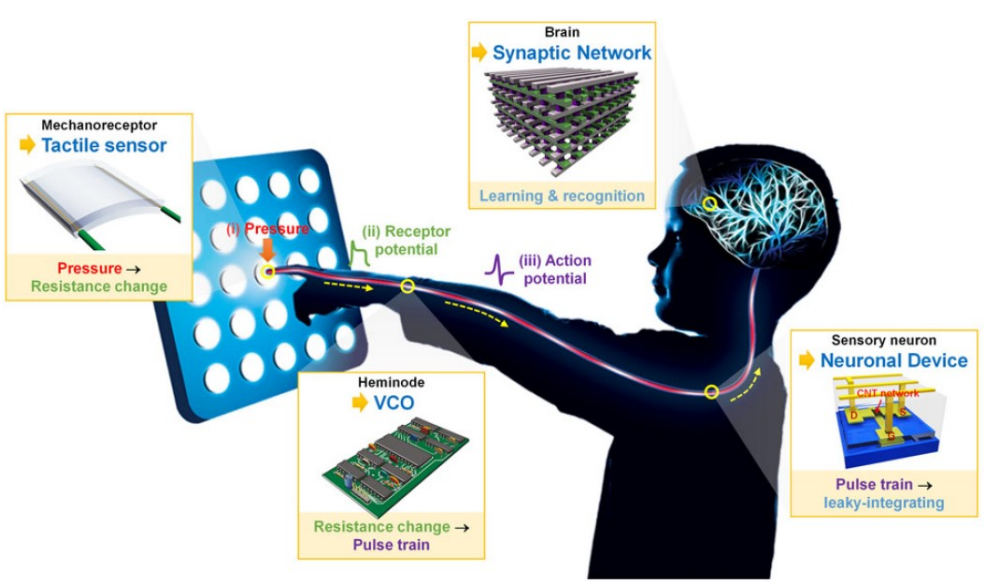


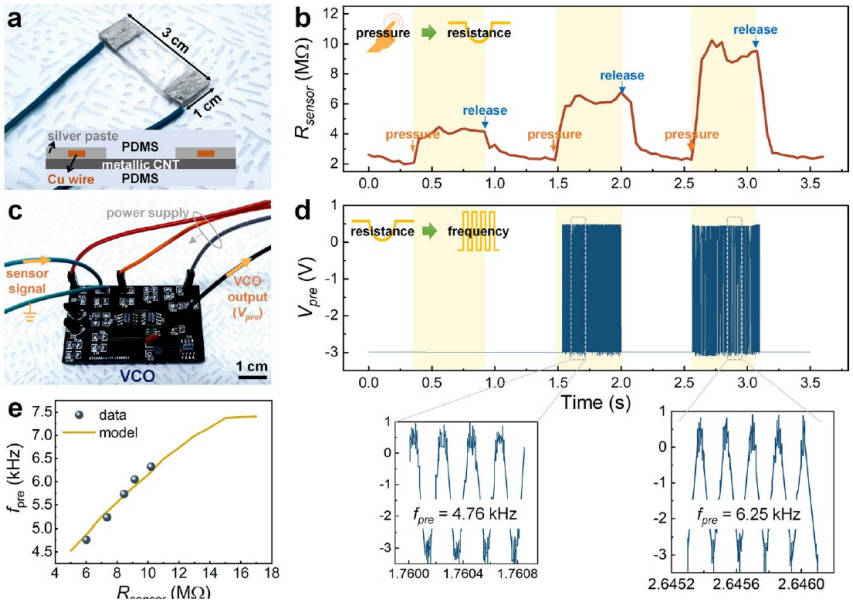


<Measurement setup>

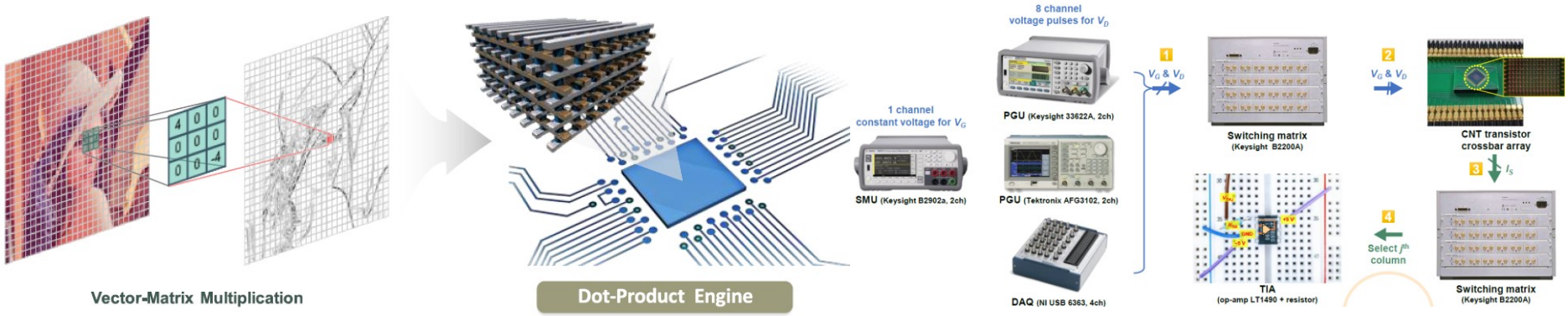
Neuromorphic System (Intelligent Semicon.)

Tactile Sensor System with sensory neurons and perceptual synaptic network



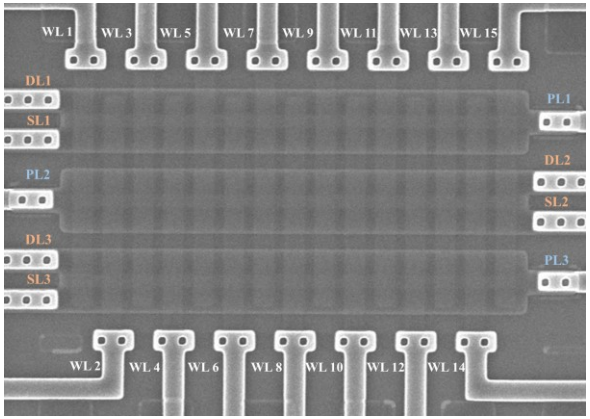


Energy-efficient vector-matrix multiplication for in-memory computing



Processing-In-Memory (PIM, Int. Semicon.)

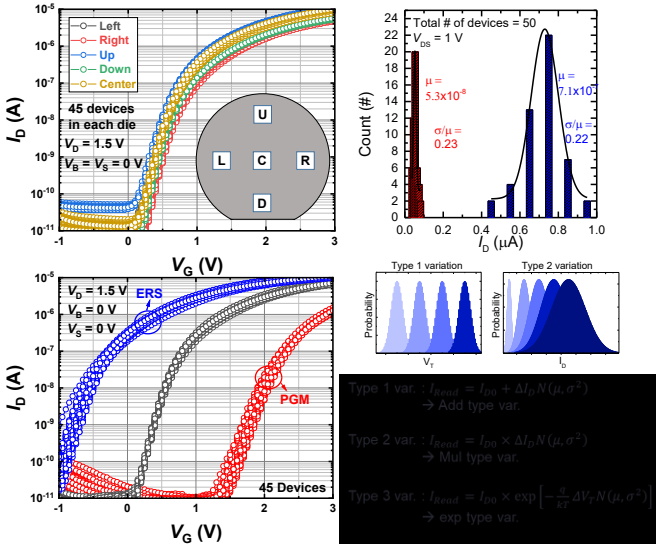
FLASH Memory Array for PIM



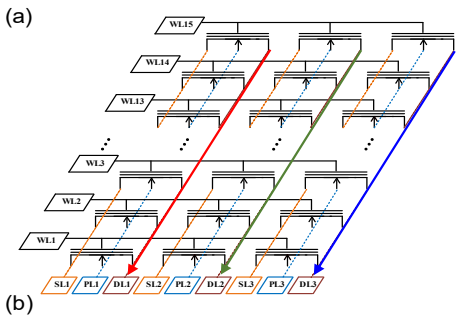
Operating Principle (Architecture Design)

	PU	Mem.	PU		Mem.	PU
Role	Input	Weighting	Weighted sum	Activation function	Weighting	Weighted sum
HW	Circuits	Memory Array	Capacitor + Circuits		Memory Array	Capacitor
Data form	V_{in} or t_{in}	$\rightarrow V_{in}Gt_{in} = Q$ (weight)	$\rightarrow \sum V_{in}Gt_{in} = \Sigma Q$	$\rightarrow V \rightarrow V_{in}$ or t_{in}	$\rightarrow V_{in}Gt_{in}$	$\rightarrow \sum V_{in}Gt_{in} = Q \rightarrow V$
SW	$a_1^{(l)}$, $a_2^{(l)}$, $a_3^{(l)}$		$\sum_{i\in l} w_{i1}^{(l)} a_i^{(l)}$, $\sum_{i\in l} w_{i2}^{(l)} a_i^{(l)}$, $\sum_{i\in l} w_{i3}^{(l)} a_i^{(l)}$	$\rightarrow f\left(s_1^{(l+1)}\right) = a_1^{(l+1)}$, $f\left(s_2^{(l+1)}\right) = a_2^{(l+1)}$, $f\left(s_3^{(l+1)}\right) = a_3^{(l+1)}$		$\sum_{j\in(l+1)} w_{j1}^{(l+1)} a_j^{(l+1)}$, $\sum_{j\in(l+1)} w_{j2}^{(l+1)} a_j^{(l+1)}$, $\sum_{j\in(l+1)} w_{j3}^{(l+1)} a_j^{(l+1)}$
	***l* layer**		***l+1* layer**			***l+2* layer**

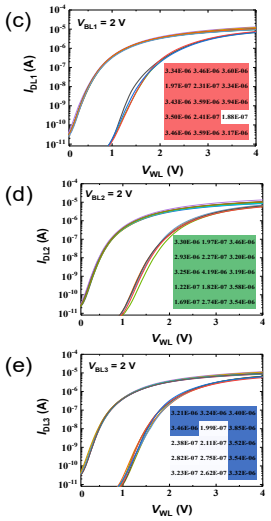
FLASH Statistical Analysis



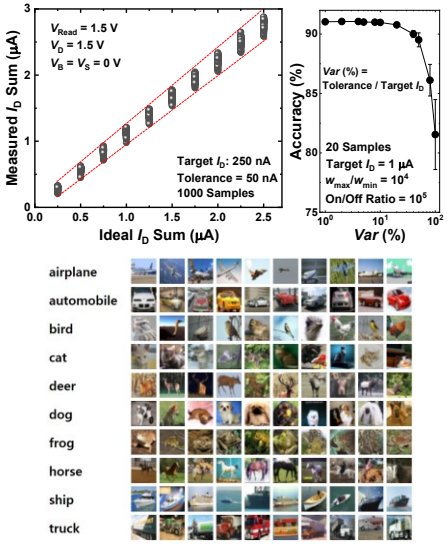
Array Architecture Design for PIM



	PGM	ERS
Select	$V_{WL} = V_{PGM}$, $V_{DL} = V_{SL} = V_{PL} = 0$ V	$V_{WL} = 0$ V, $V_{DL} = V_{SL}$ = floating, $V_{PL} = V_{ERS}$
Unselect	$V_{WL} = 0$ V or $V_{DL} = V_{SL}$ = floating, $V_{PL} = V_{INH1}$	$V_{WL} = V_{INH2}$ or $V_{DL} = V_{SL}$ = floating, $V_{PL} = 0$ V

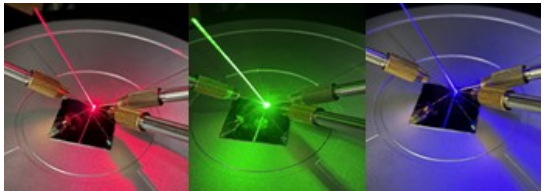


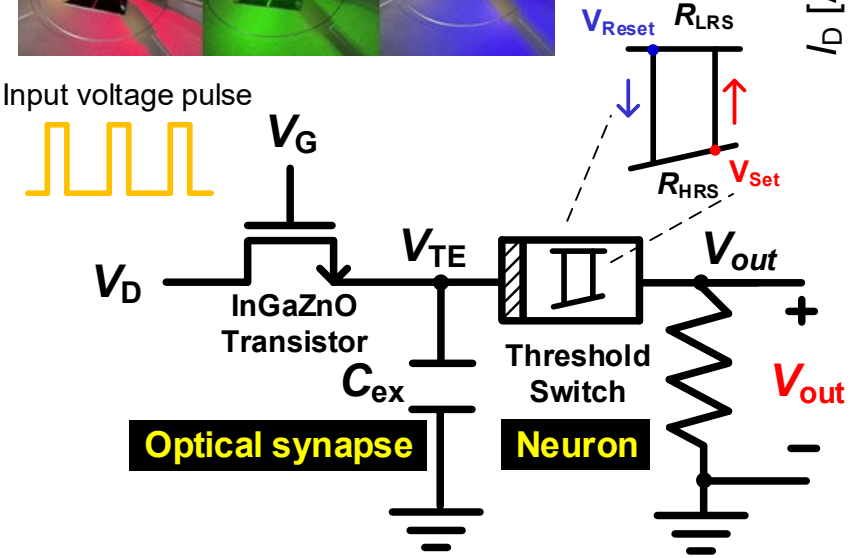
Operating Accuracy

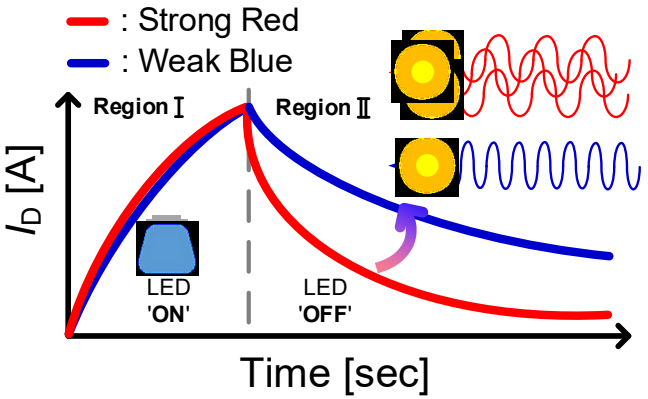


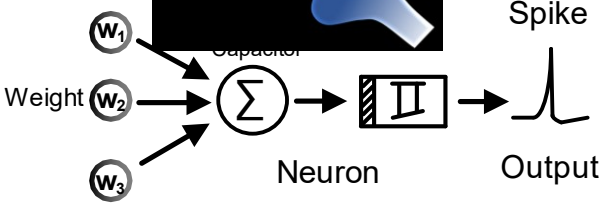
Circadian Rhythm-Based Wearable Healthcare

Leaky Integrate & Fire Neuron Circuit for Circadian Rhythm Diagnosis





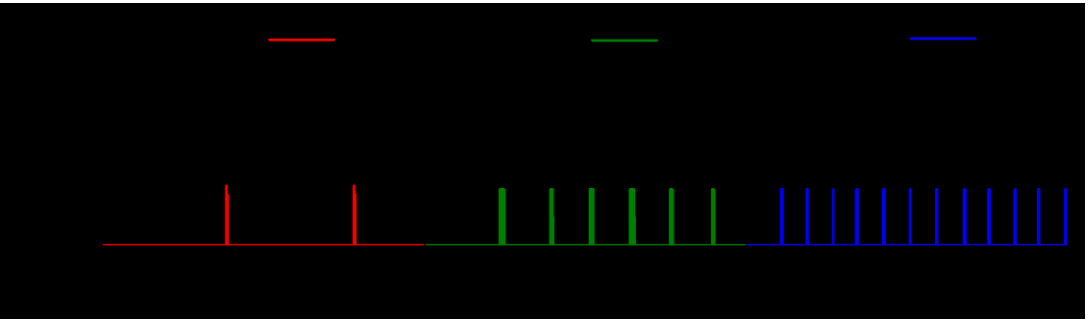


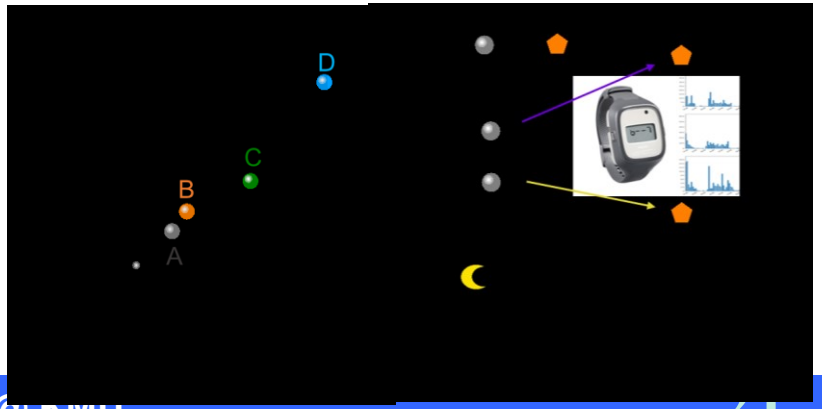


Measuring HRV

Measuring EEG

Spiking numbers with RGB light





Summary

연구분야 : 반도체 기술 전반 (재료, 소자, 공정, 회로, 시스템)

응용분야 : **1) 상용 기술** 개선 / **차세대 기술** 개발 (메모리/비메모리)

2) AI 반도체, 스마트 IoT 기기 및 **스마트 시스템** 개발

(로직, 메모리, 디스플레이, 센서 etc.)

기술구분 :

* **소자 설계** (구조, 재료, 성능 확보 목표 (**실용적 기술** 지향))
* **공정 설계** (Process Design)
* **공정 기술/소자 제작** (Device Fabrication)
* **소자 분석** (측정, 분석, 시뮬레이션)
* **응용을 위한 반도체 회로 및 시스템**

산학협력 (반도체전공트랙 참여기관) :

* **SAMSUNG, LG, ㈜AIsemy, ㈜써카디언, 등.** (확대 계획)