연구실 소개

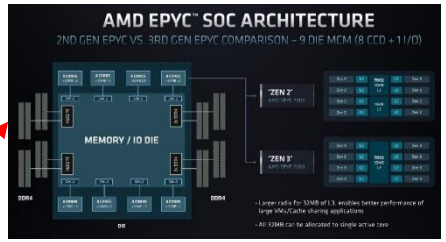
SeDA
Semiconductor Design
Automation Laboratory

반도체설계자동화연구실
(Semiconductor Design Automation Lab.)

지도교수: 박희천

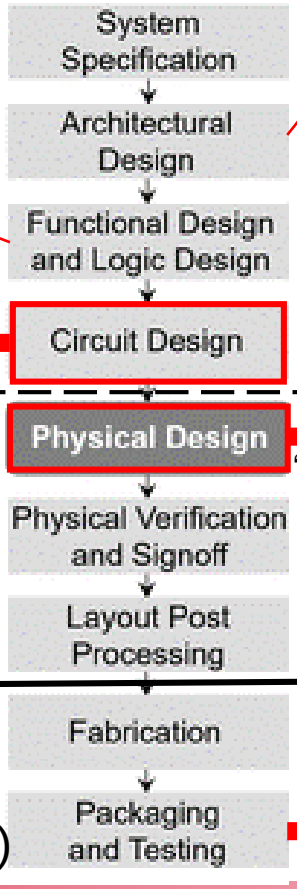
SeDA
Semiconductor Design Automation Laboratory

- 시스템반도체 설계 자동화 & 최적화
  - VLSI (초고밀도 집적회로) & SoC (단일 칩 시스템)
  - EDA (전자설계자동화), CAD (컴퓨터이용설계)



▲ System architecture

▼ VLSI EDA flow



▼ RTL (Register-transistor level)

```
input clk, rst;
input [63:0] A, B, C, D, E, F;
input Cin;
output reg [63:0] S;
output reg Cout;

reg [63:0] S1, S2, S3, S4;
reg Cout1, Cout2, Cout3, Cout4;

always @(posedge clk or posedge rst) begin
    if (rst) begin
        S <= 63'b0;
        S1 <= 63'b0;
```

▼ Gate-level netlist

```
      n66247) );
XOR2xp5_ASAP7_75t_R U65005 ( .A(n30906), .B(n70177), .Y(n70
XNOR2xp5_ASAP7_75t_R U65006 ( .A(n31174), .B(n70945), .Y(n7
AOI22xp5_ASAP7_75t_R U65007 ( .A1(n62051), .A2(n62050), .B
      n62048), .Y(n62052) );
OAI21xp5_ASAP7_75t_R U65008 ( .A1(n67276), .A2(n67275), .B
      n67277) );
XNOR2xp5_ASAP7_75t_R U65009 ( .A(n31416), .B(n71224), .Y(n7
AOI31xp33_ASAP7_75t_R U65010 ( .A1(n67015), .A2(n67014), .
      n67012), .Y(n67016) );
OAI22xp5_ASAP7_75t_R U65011 ( .A1(n60266), .A2(n60265), .B
```

Logic Synthesis

Standard cells

```
      n66247) );
XOR2xp5_ASAP7_75t_R U65005 ( .A(n30906), .B(n70177), .Y(n70
XNOR2xp5_ASAP7_75t_R U65006 ( .A(n31174), .B(n70945), .Y(n7
AOI22xp5_ASAP7_75t_R U65007 ( .A1(n62051), .A2(n62050), .B
      n62048), .Y(n62052) );
OAI21xp5_ASAP7_75t_R U65008 ( .A1(n67276), .A2(n67275), .B
      n67277) );
XNOR2xp5_ASAP7_75t_R U65009 ( .A(n31416), .B(n71224), .Y(n7
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      n67012), .Y(n67016) );
OAI22xp5_ASAP7_75t_R U65011 ( .A1(n60266), .A2(n60265), .B
```
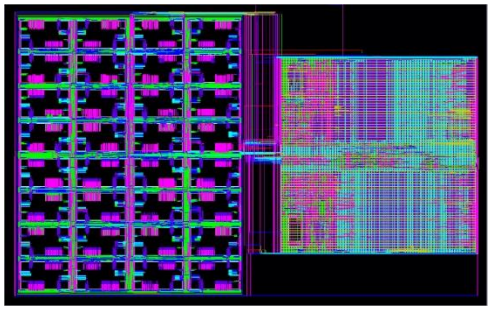

▲ Gate-level netlist

"logical"

"physical"

Place & Route (P&R)



▲ GDS (Graphic design system)

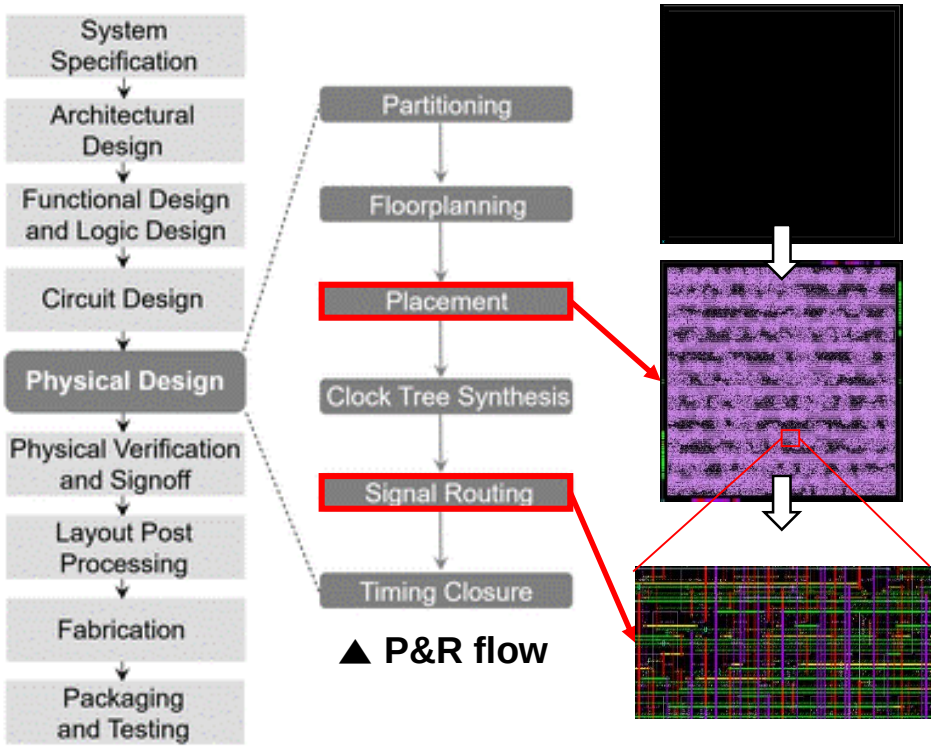
설계

생산 (공정)

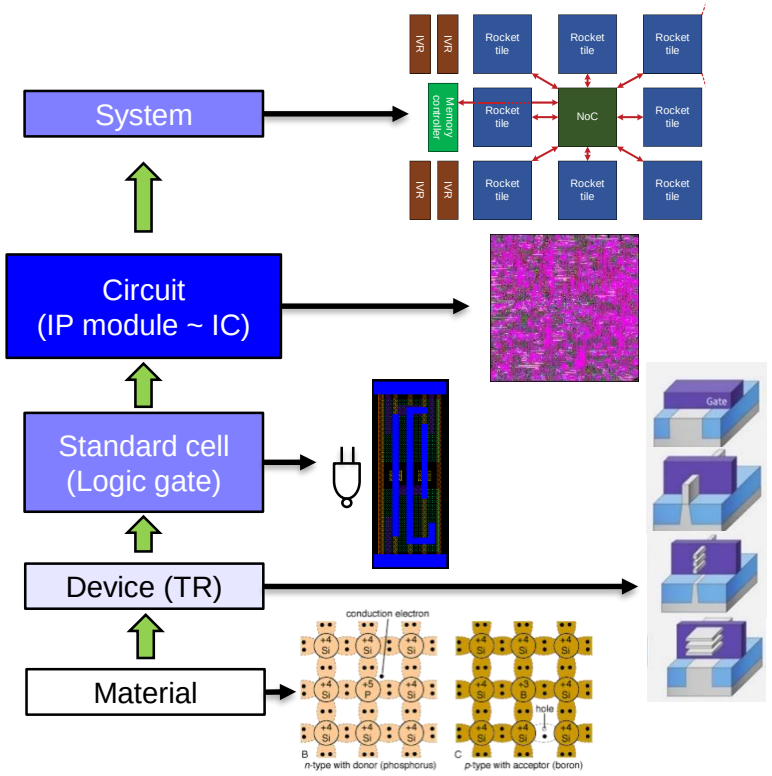
◀ Wafer

연구 분야

- Place & Route 알고리즘 개선 및 개발
- 설계 자동화&최적화 대상: Standard cell ~ **IC** ~ System



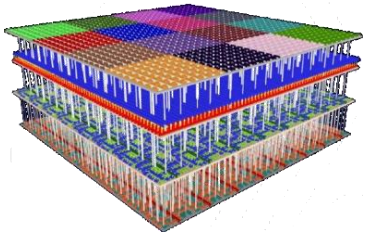
▲ **P&R flow**

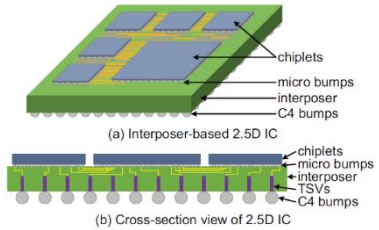


세부 주제

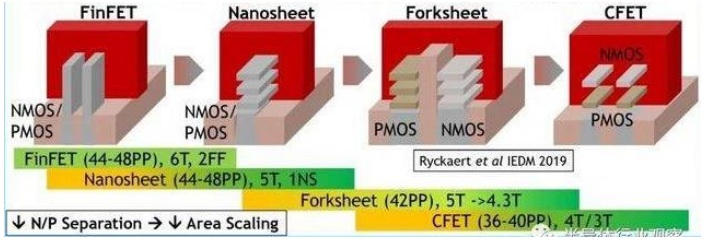
Next-generation architecture

- 새로운 구조/공정 반도체 설계



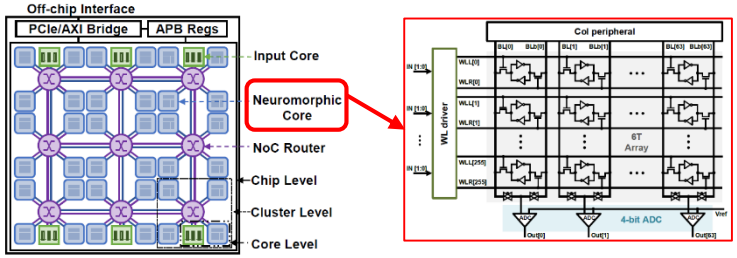


Advanced design environment

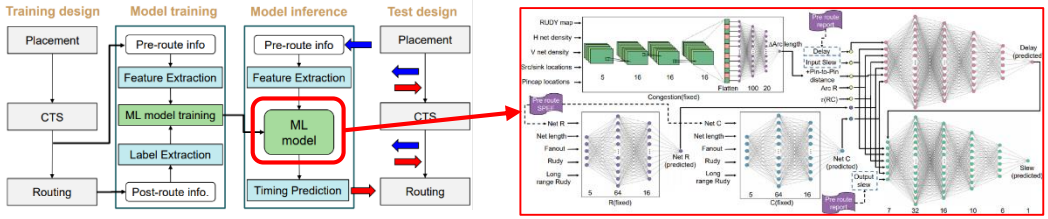


Intelligent SoC/VLSI

- 설계 자동화 ↔ 인공지능



Machine learning for EDA



연구 계획

- **~23.2**: EDA flow 및 design stage 학습
- **23.3 ~ 23.6**: EDA tool 사용
- **23.7 ~ (?)**: 세부 주제 학습 및 연구
  - 수직적층 구조 → EDA for 3D/2.5D design
  - 최신 공정 & design rules → design-rule-aware EDA
  - Memory → PIM 구조 → EDA for PIM architecture
  - CPU architecture → neuromorphic → physical design (EDA) for NPU
  - ML → Early-stage design prediction & optimization
  - ML & RL → RL-based design automation
  - ……

	SYNOPSYS	cadence
Synthesis	**Design Compiler**	**Genus**
Place & Route	**IC Compiler**	**Innovus**
Signoff Analysis	**PrimeTime,** PrimeRail, …	**Tempus,** Voltus, …

[산학 컨소시엄 참여기업 현황]

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시스템응용 (6)	㈜Solum(기흥) Inter M(경기 양주) ㈜성호전자(가산) JPI Healthcare ㈜(방배) ㈜이엠이코리아(대구) ㈜케이엠더블류(화성시)
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Thank you!

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